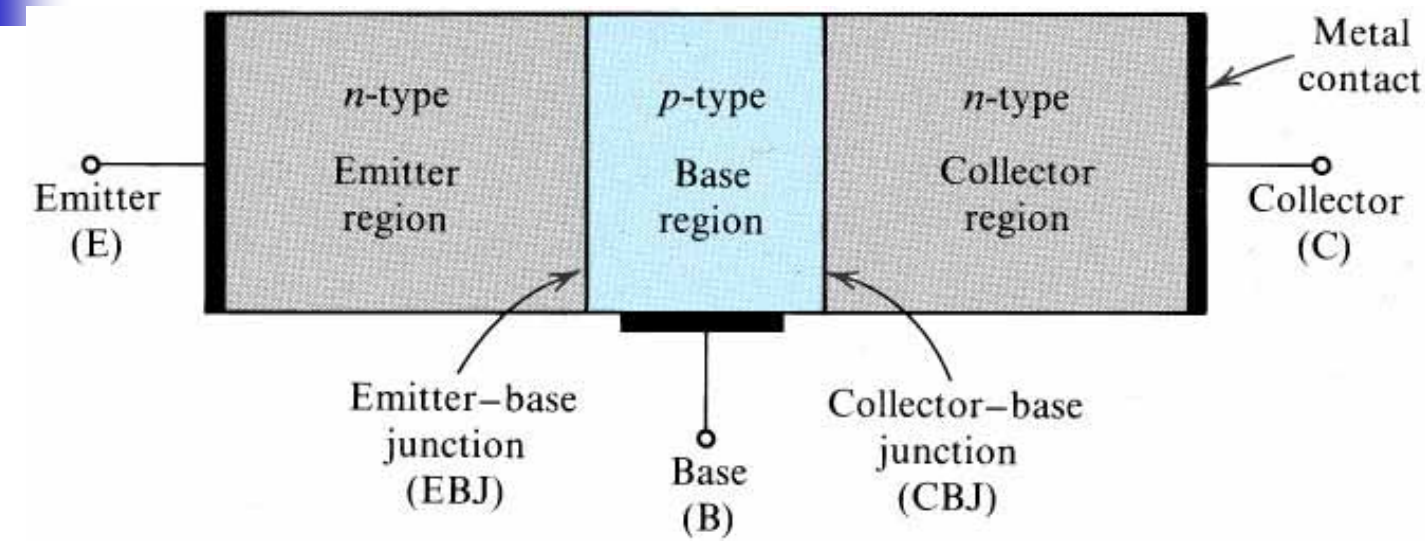
Chapter 2 :
Semiconductor Materials & Devices (II)

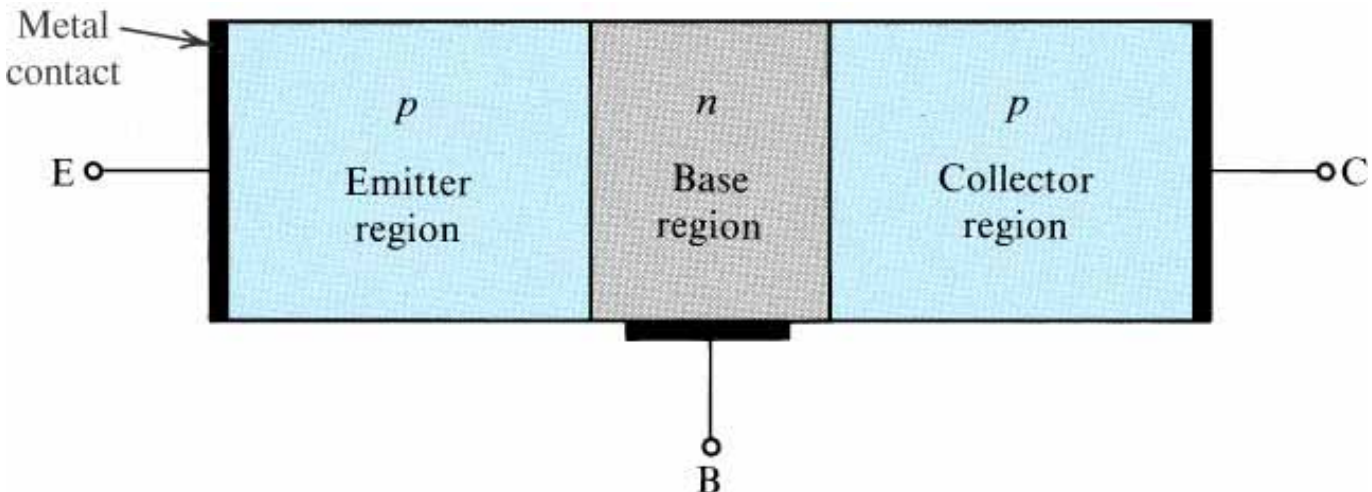
Feb. 2005
中山電機系　黃義佑

Reference

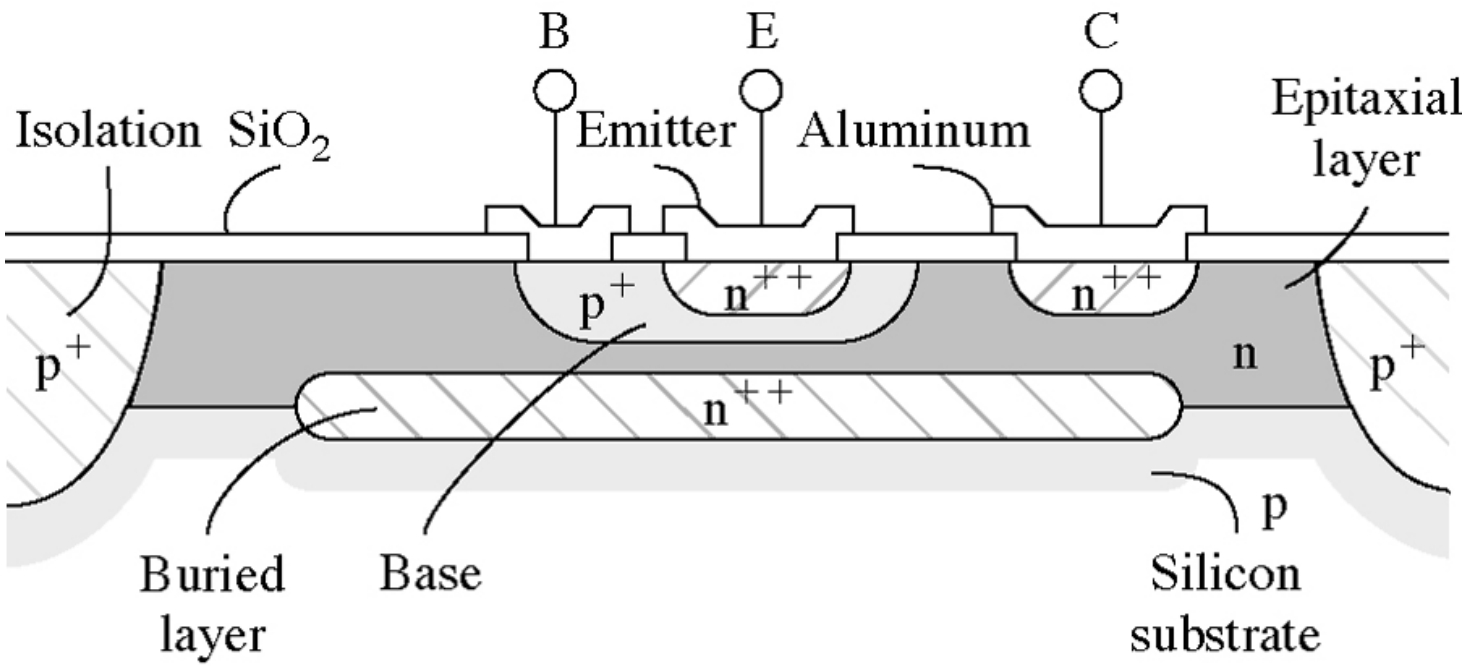
1. SemiconductorManufacturing Technology*: Michael Quirk and Julian Serda (2001)*
2. 國家矽導計畫-教育部晶片法商學程編定教材
3. Microelectronic Circuits (5/e): Sedra & Smith (2004)
4. Semiconductor Physics and Devices- Basic Principles (3/e) *: Donald A. Neamen (2003)*
5. Semiconductor Devices - *Physics and Technology* (2/e) *: S. M. Sze (2002)*

Bipolar Junction Transistor





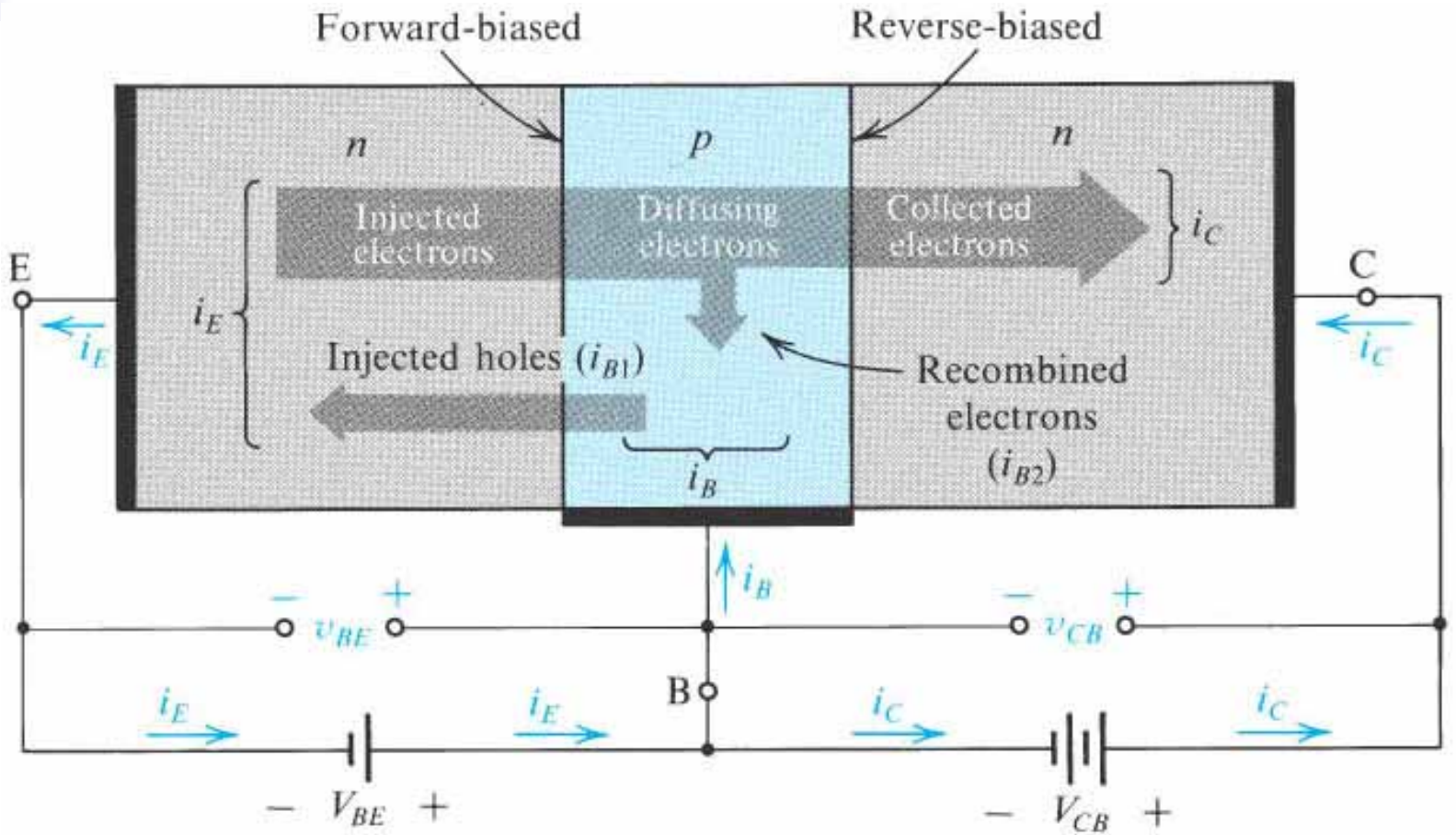
Cross Section of an NPN BJT



Conventional npn transistor

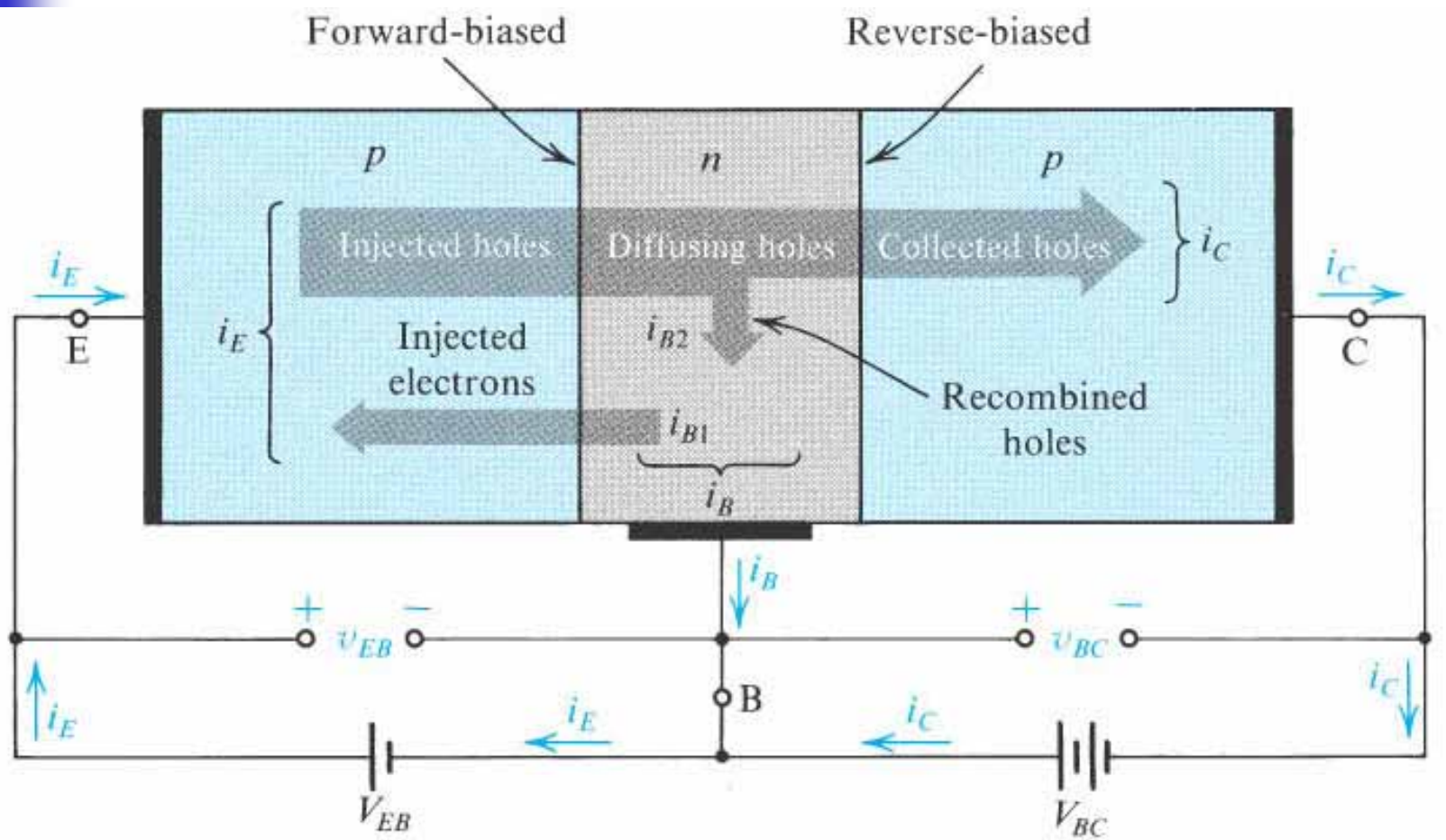
BJT is not a symmetrical device and the impurity doping concentrations in the emitter and collector are different.

NPN Transistor Biasing Circuit



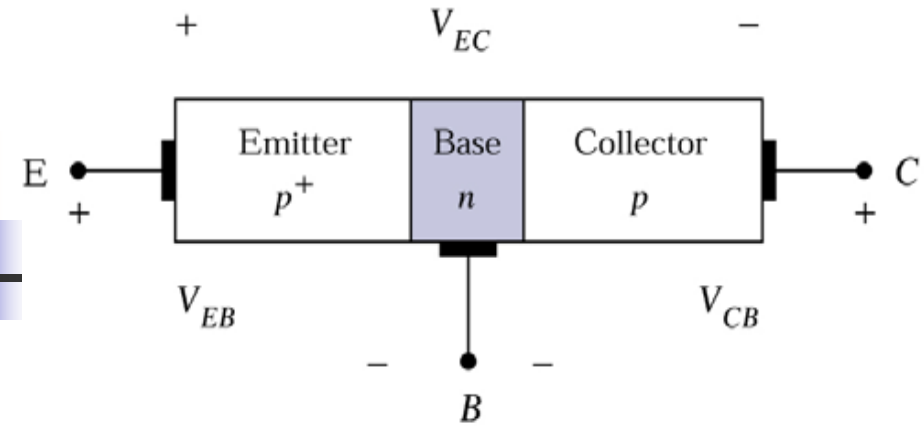
Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

PNP transistor biasing circuit

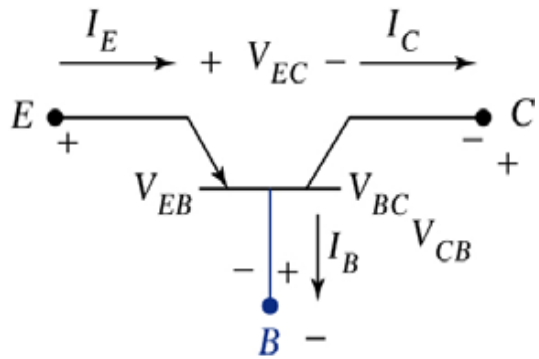


Current flow in a *pnp* transistor biased to operate in the active mode.

The Transistor Action

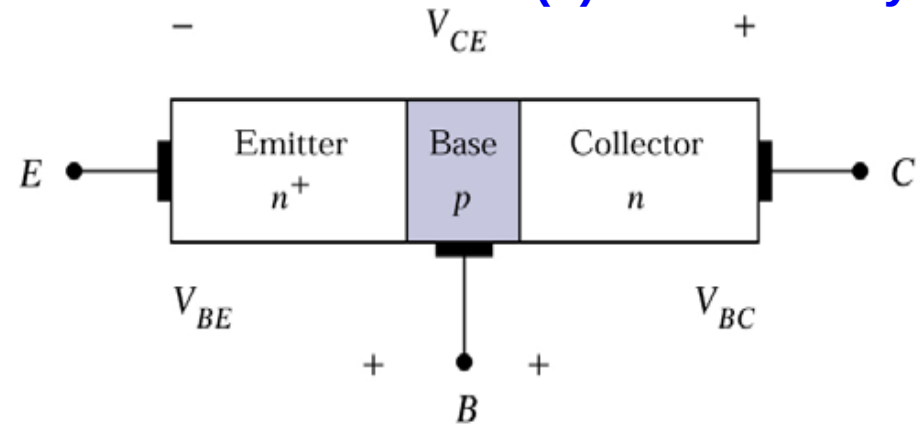


(a)

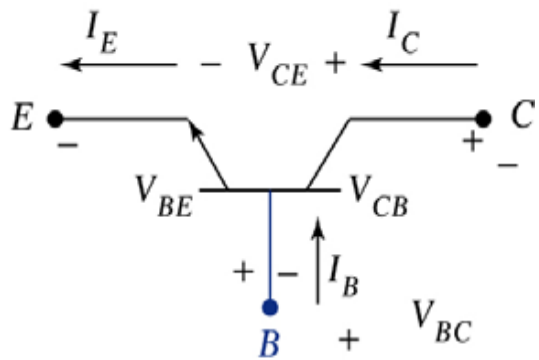


(b)

(a) Idealized one-dimensional schematic of a *p-n-p* bipolar transistor and (b) its circuit symbol.



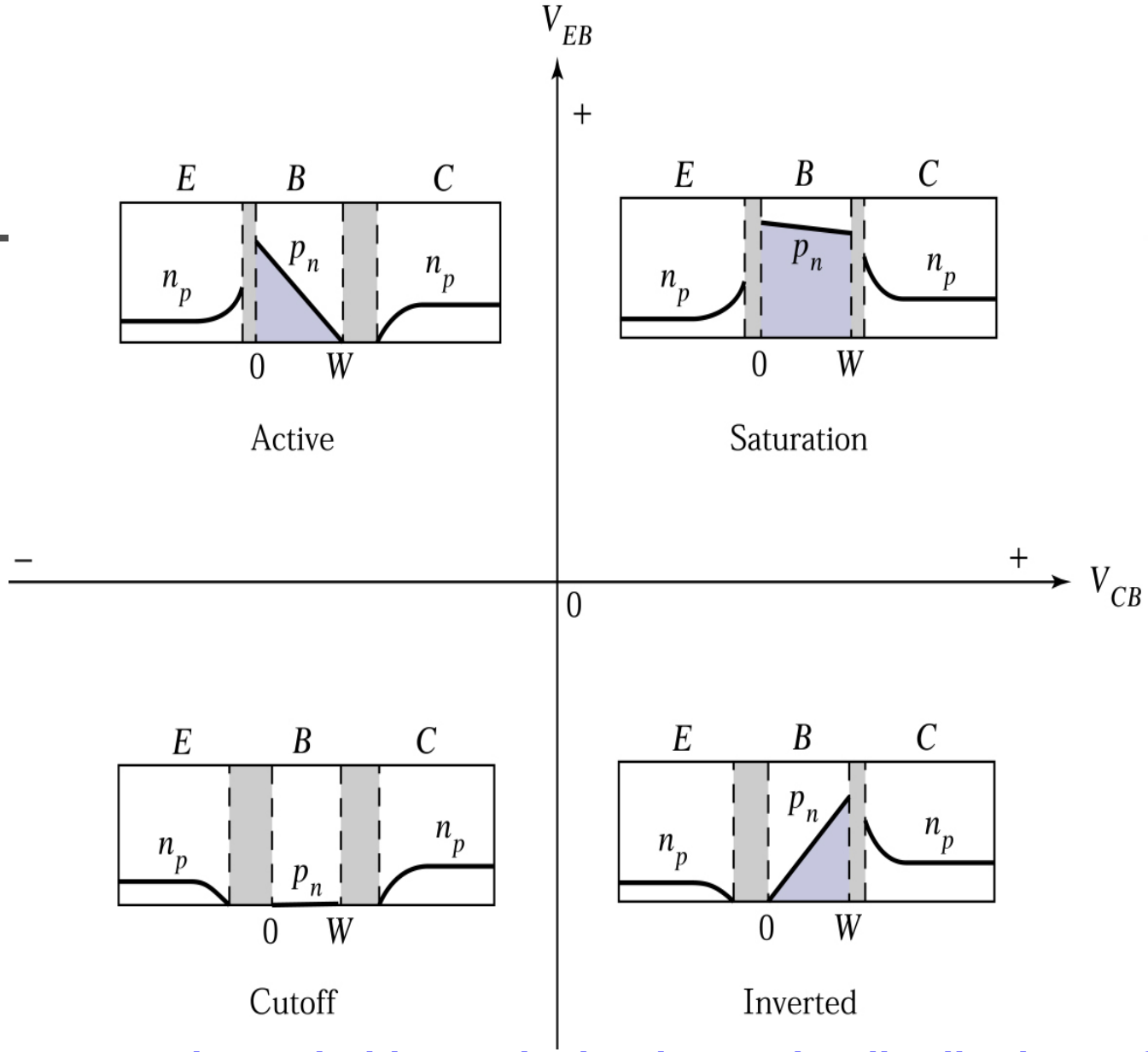
(c)



(d)

(*c*) Idealized one-dimensional schematic of an *n-p-n* bipolar transistor (*d*) its circuit symbol.

Modes of Operation



Junction polarities and minority carrier distributions of a p-n-p transistor under four modes of operation.

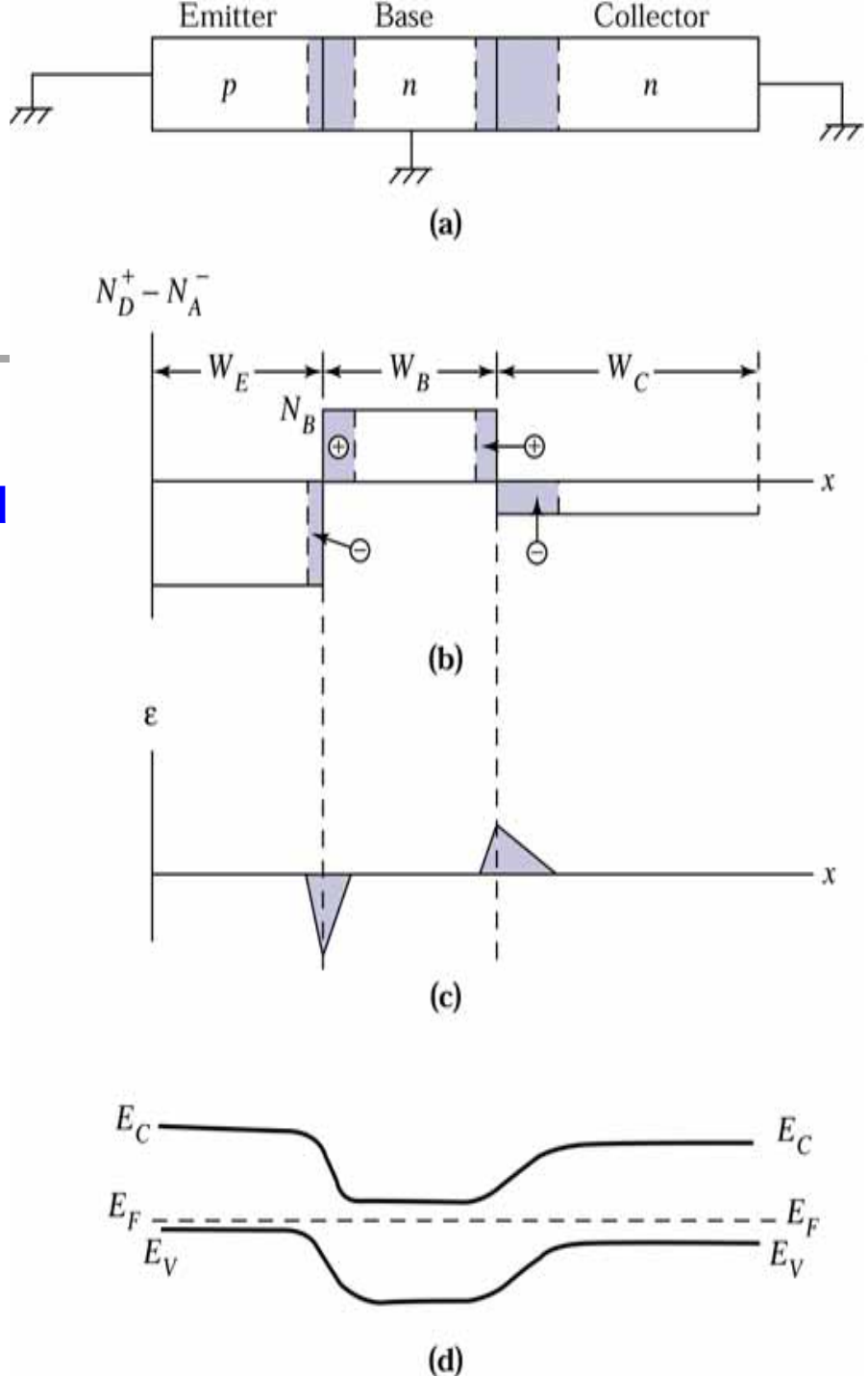
Operation in the Thermal Equilibrium

(a) A *p-n-p* transistor with all lead grounded (at thermal equilibrium).

(b) Doping profile of a transistor with abrupt impurity distributions.

(c) Electric-field profile.

(d) Energy band diagram at thermal equilibrium.



Operation in the Active Mode

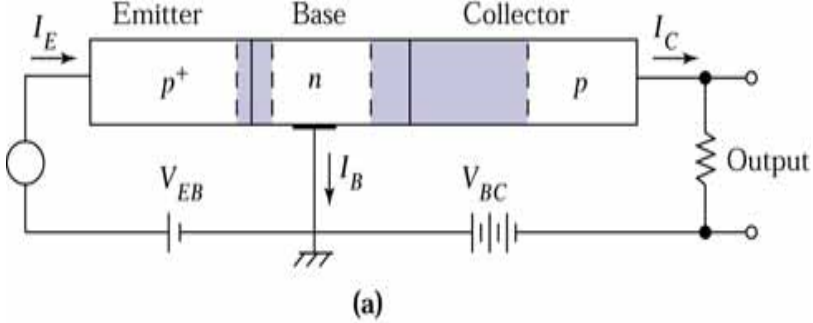
Common-base (CB) configuration

(a) The transistor under the active mode of operation.

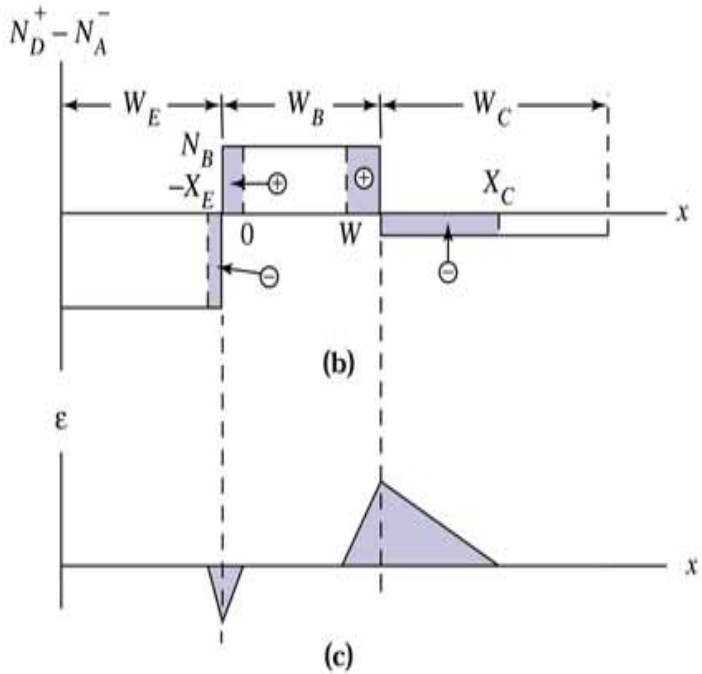
(b) Doping profiles and the depletion regions under biasing conditions.

(c) Electric-field profile.

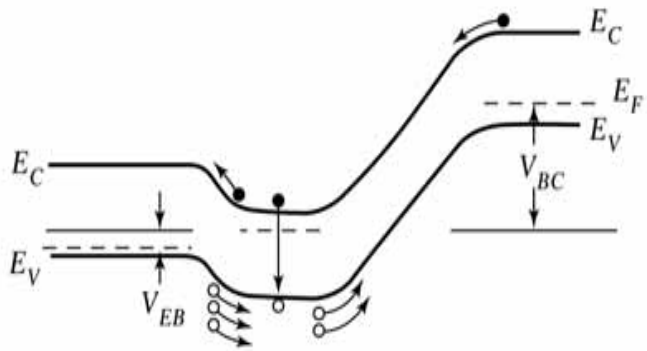
(d) Energy band diagram.



(a)



(c)



(d)

Current Gain

Common-base configuration

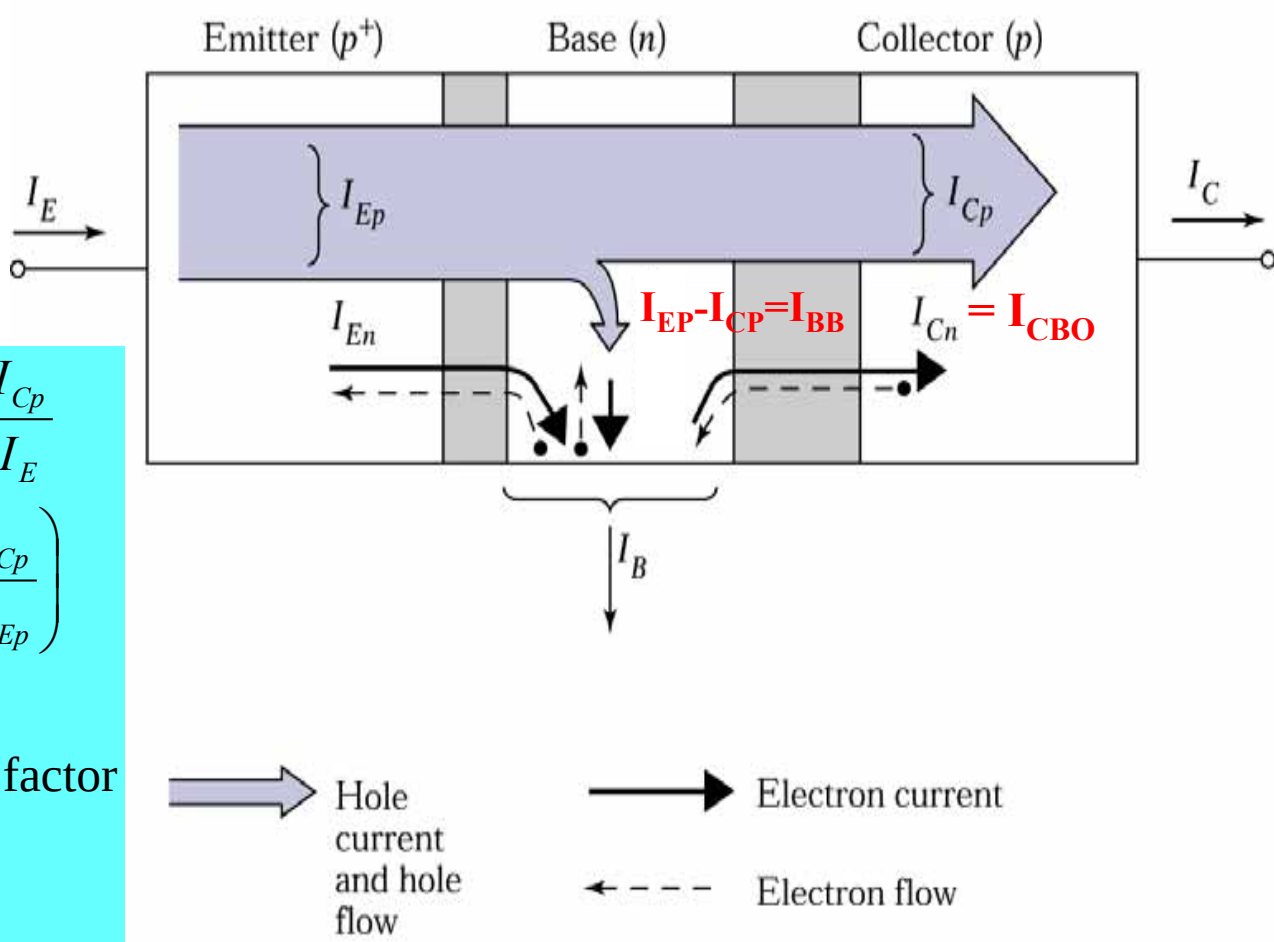
$$I_E = I_{Ep} + I_{En}$$
$$I_C = I_{Cp} + I_{Cn}$$
$$I_B = I_E - I_C$$
$$= I_{En} + (I_{Ep} - I_{Cp}) - I_{Cn}$$

$$\text{common-base current gain } \alpha_0 \equiv \frac{I_{Cp}}{I_E}$$

$$\Rightarrow \alpha_0 = \frac{I_{Cp}}{I_{Ep} + I_{En}} = \left(\frac{I_{Ep}}{I_{Ep} + I_{En}}\right)\left(\frac{I_{Cp}}{I_{Ep}}\right)$$
$$= \gamma \alpha_T$$

γ : emitter eff. α_T : base transport factor

$$\Rightarrow I_C = I_{Cp} + I_{Cn} = \alpha_T I_{Ep} + I_{Cn}$$
$$= \alpha_0 I_E + I_{CBO}$$

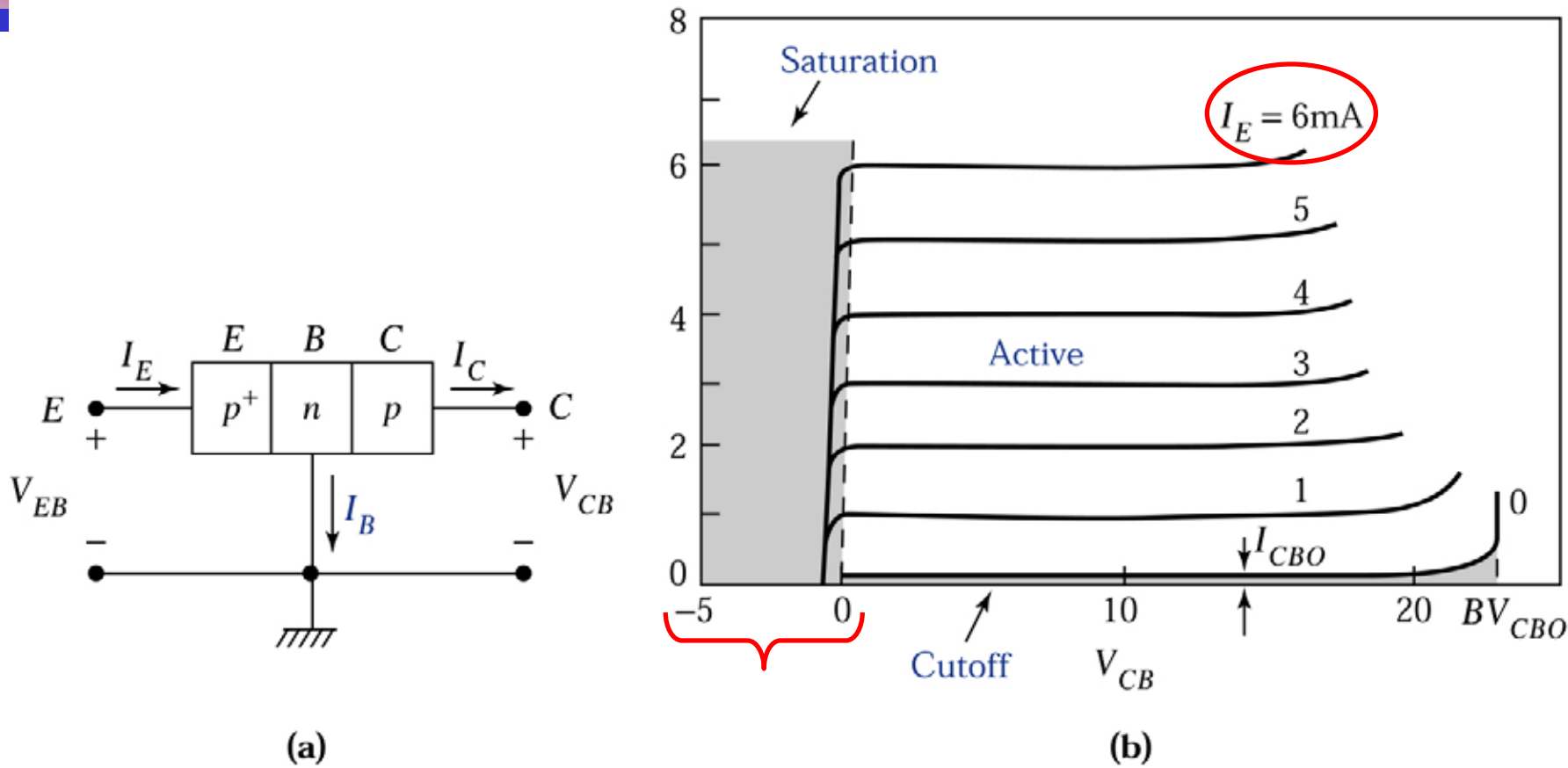


Various current components in a *p-n-p* transistor under active mode of operation. The electron flow is in the opposite direction to the electron current.

Feb. 2005
中山電機系　黃義佑

Current-Voltage Characteristics

Common-base configuration



(a) Common-base configuration of a *p-n-p* transistor.

(b) Its output current-voltage characteristics.

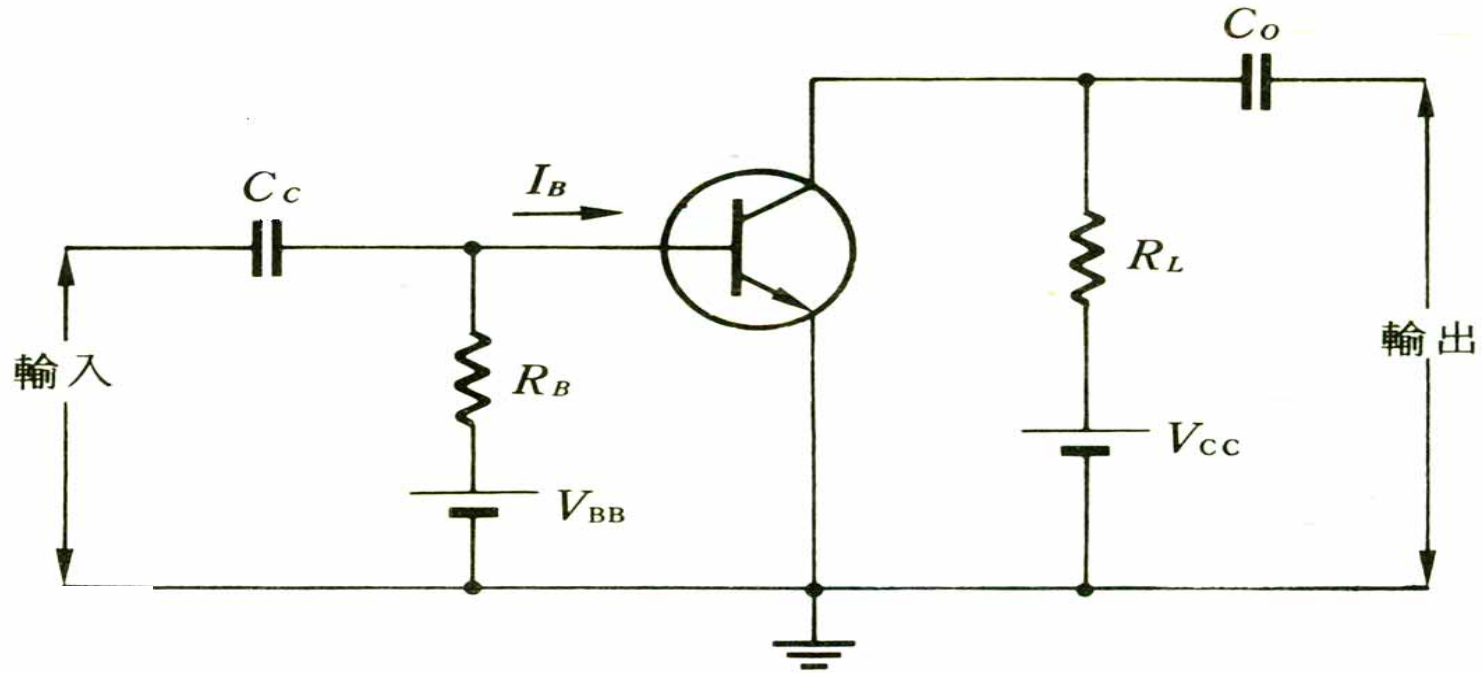
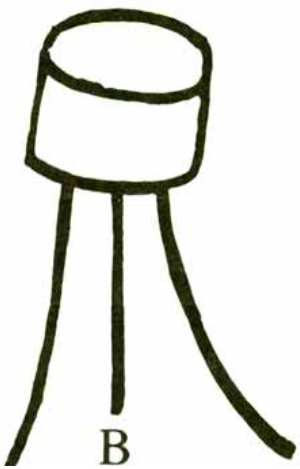


圖 5-1　共射極放大器之基本電路



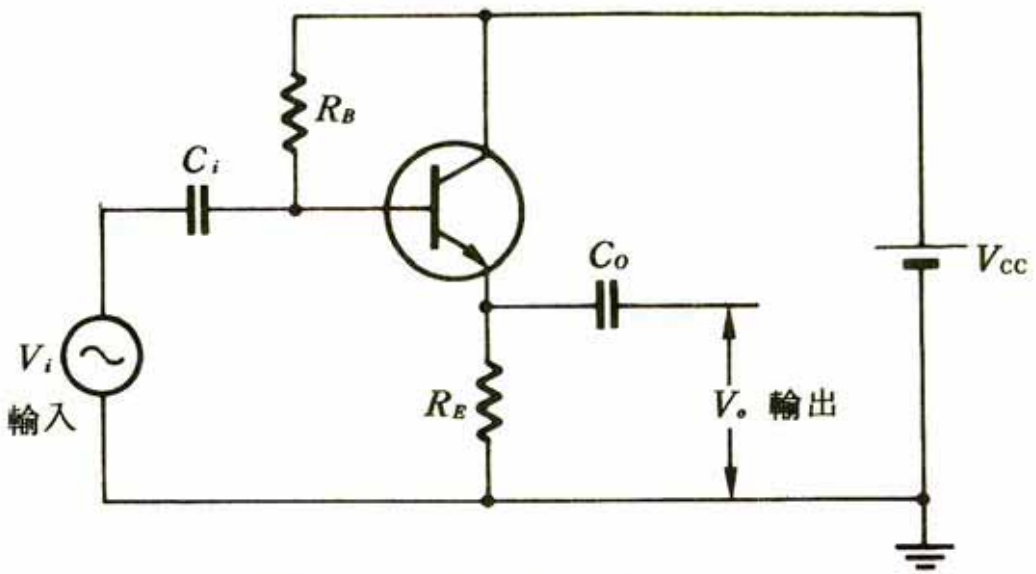
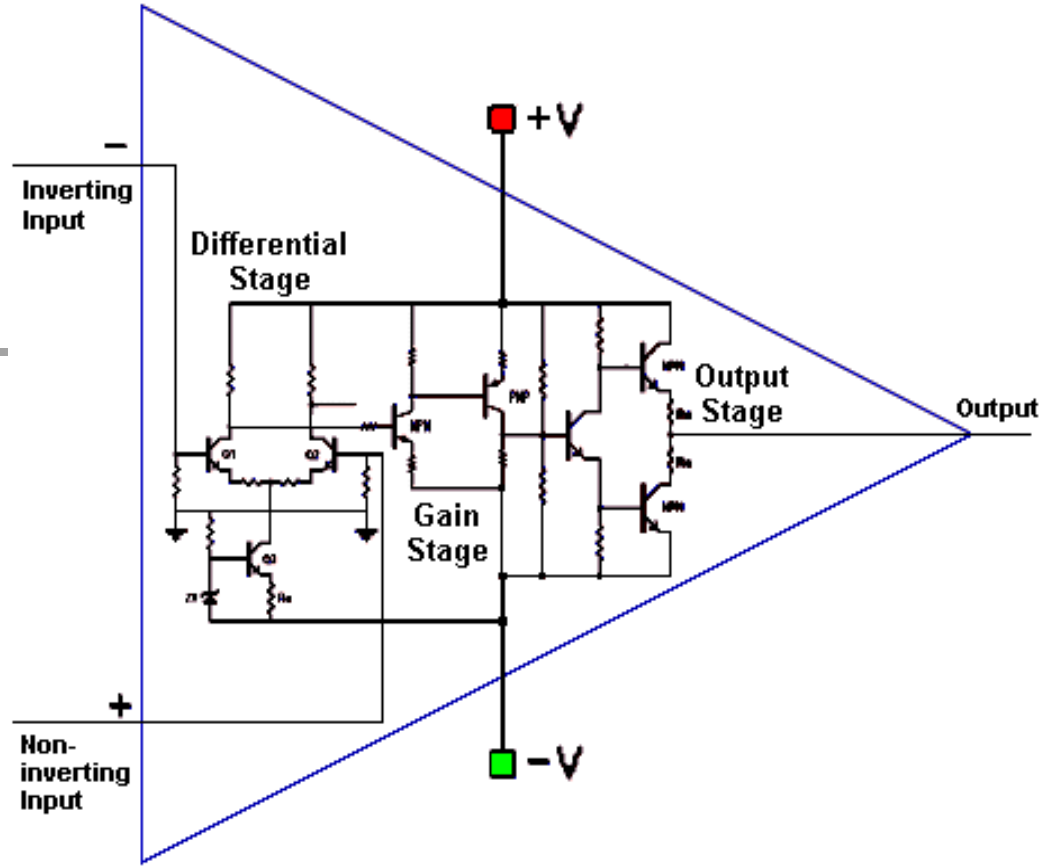


圖 7-1　共集極放大器之基本電路

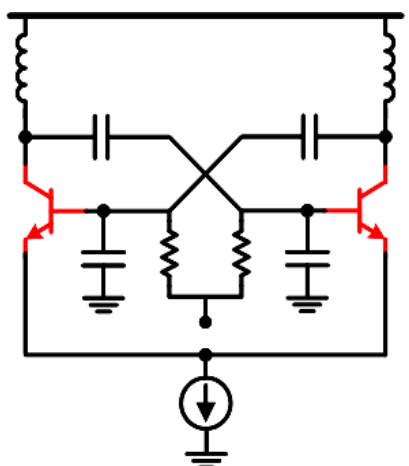
CE、CC、CB放大器之特性比較

	共射極（CE）	共集極（CC）	共基極（CB）
輸入端	基極	基極	射極
輸出端	集極	射極	集極
共用端	射極	集極	基極
輸入電阻	中	高	低
輸出電阻	中	低	高
電壓增益	大	略小於 1	大
電流增益	大	大	略小於 1
功率增益	最大	大	大
V_i與V_o之相位關係	180度（反相）	0度（同相）	0度（同相）

Applications



- **Advantage**
  - High operating speed
  - High driving current
- **Analog Circuits**
  - Amplifier
  - RF circuits
  - Automobile electronics



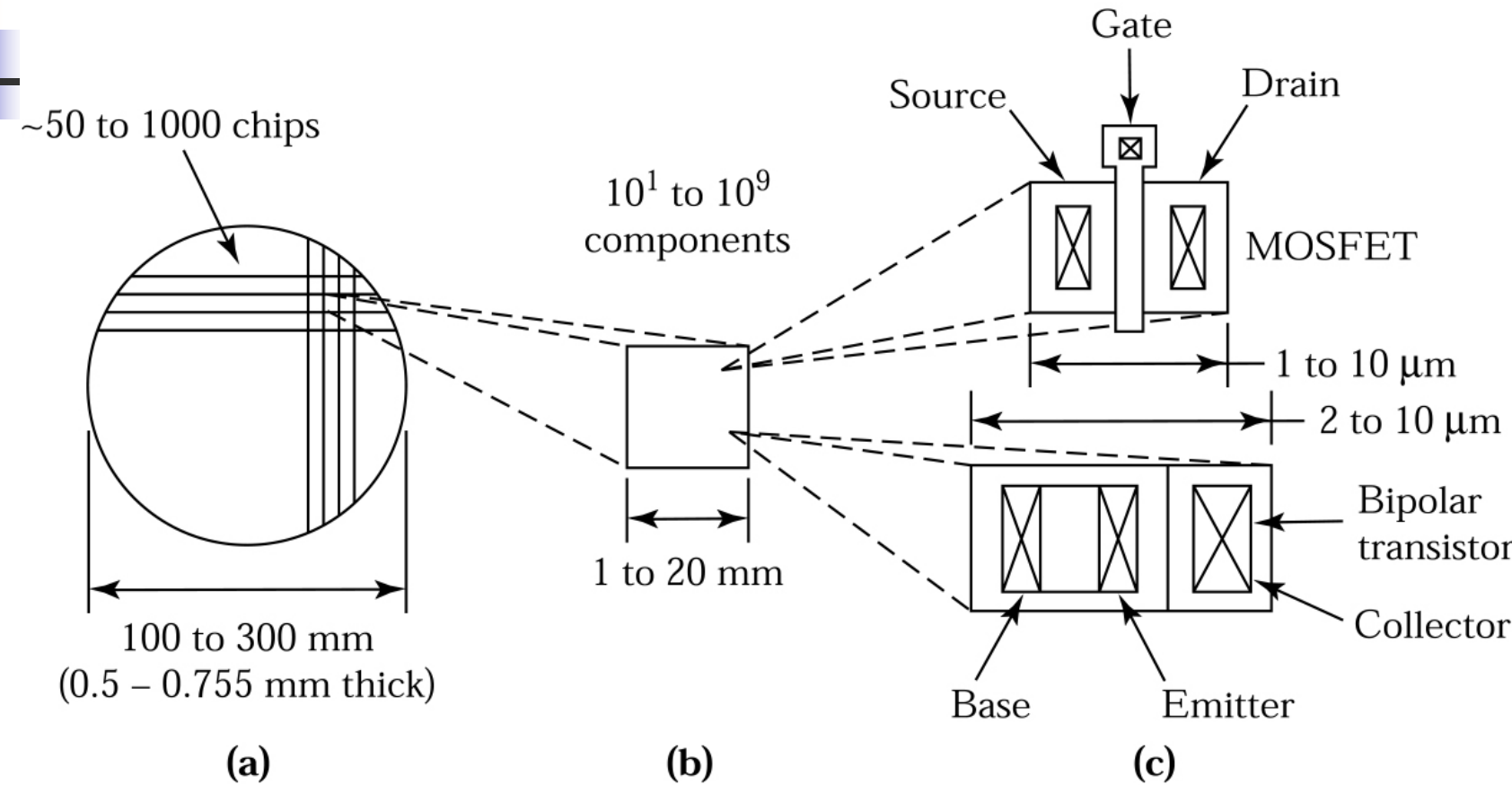
Bipolar Logic Families

Table 3.1 Bipolar Logic Families	
Bipolar Logic Family	**Abbreviation**
Direct-Coupled Transistor Logic	DCTL[1]
Resistor-Transistor Logic	RTL[2]
Resistor-Capacitor-Transistor Logic	RCTL[3]
Diode-Transistor Logic	DTL[4]
Transistor-Transistor Logic*	TTL[5]
Schottky TTL Logic*	STTL[6]
Emitter-Coupled Logic*	ECL[7]

---

[1] G. Deboo and C. Burrous, *Integrated Circuits and Semiconductor Devices: Theory and Application*, 2nd edition, McGraw-Hill, New York, NY, 1977, p. 192.
[2] G. Deboo and C. Burrous, ibid.
[3] G. Deboo and C. Burrous, ibid.
[4] G. Deboo and C. Burrous, ibid.
[5] G. Deboo and C. Burrous, ibid.
[6] A. Sedra, K. Smith, *Microelectronic Circuits*, Oxford University Press, 1998, p. 1187.
[7] A. Sedra, K. Smith, *Microelectronic Circuits*, Oxford University Press, 1998, p. 1196.

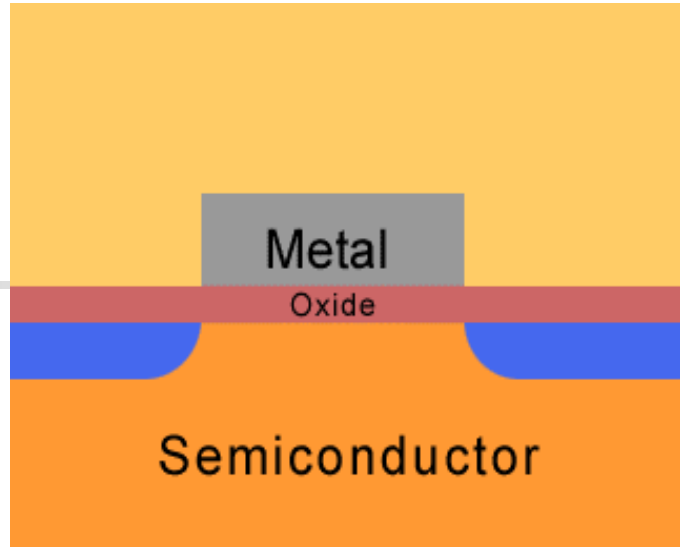
Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

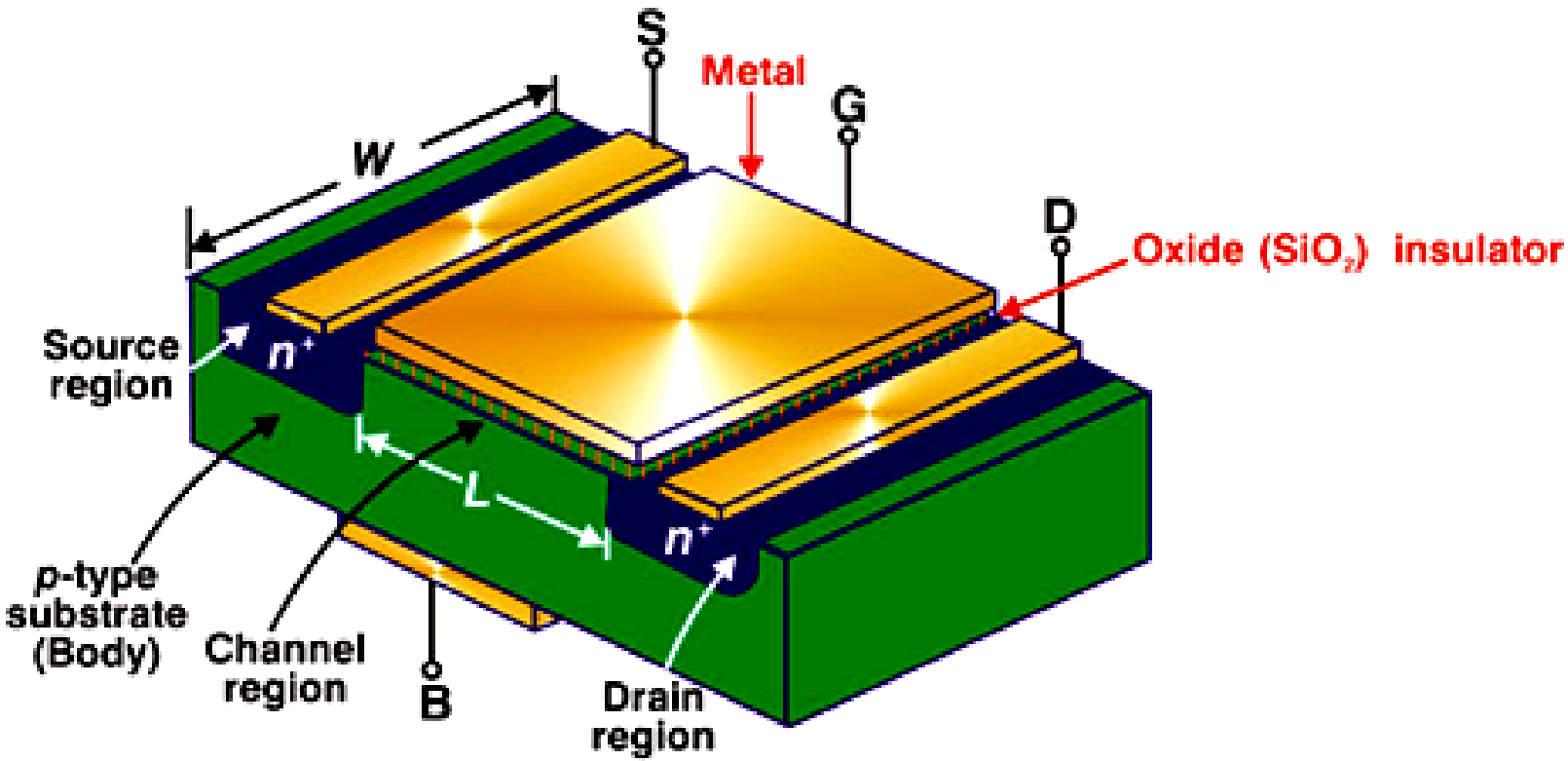


Size comparison of a wafer to individual components. (*a*) Semiconductor wafer. (*b*) Chip. (*c*) MOSFET and bipolar transistor.

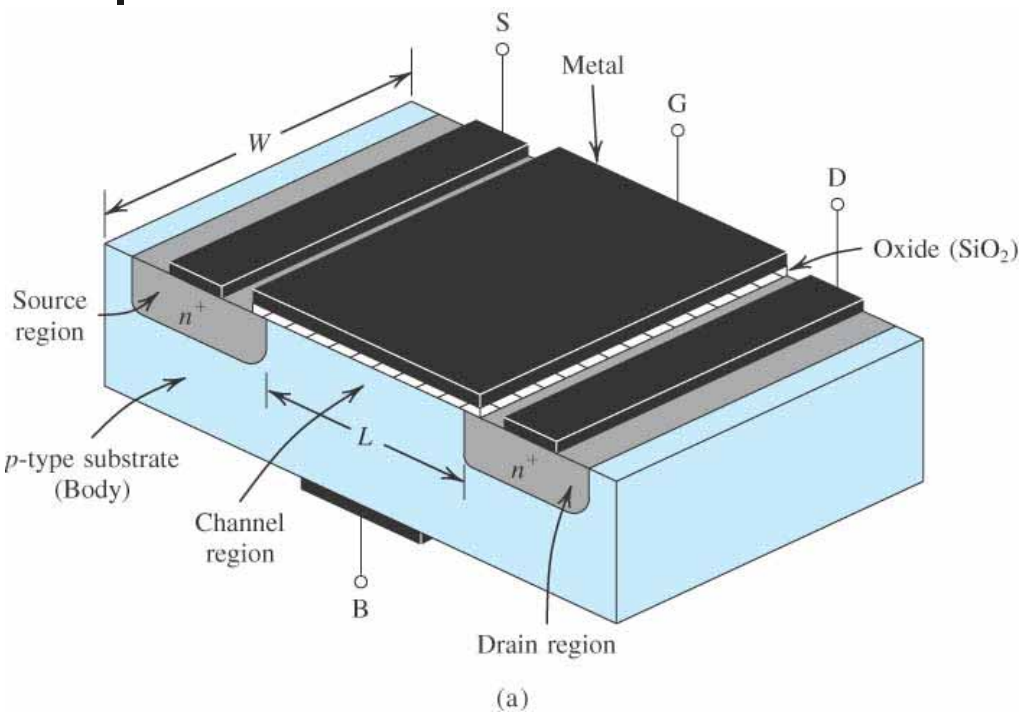
Structure of MOSFET

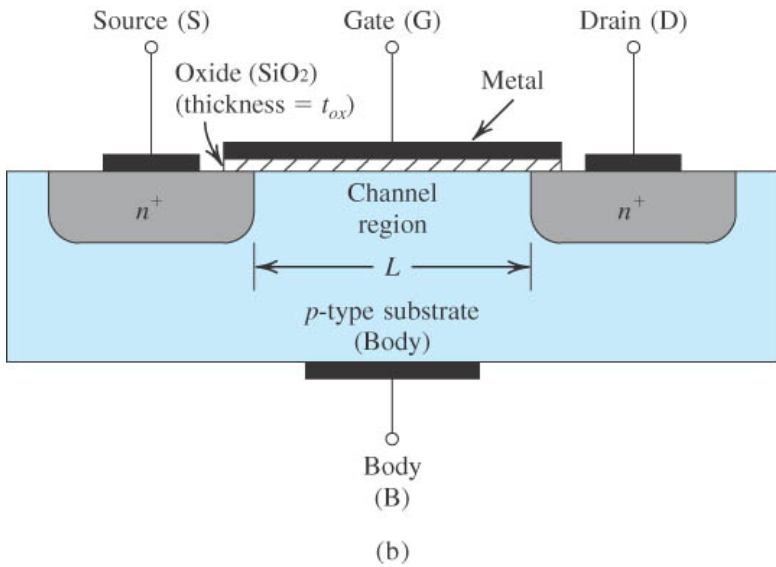
- **Gate**
  - Metal (Aluminum) → polysilicon
  - Oxide – thickness of *tox*
- **Source** and **Drain**
  - Two heavily doped regions
- **Body or substrate** (“bulk” or “body”)
  - Lightly doped substrate





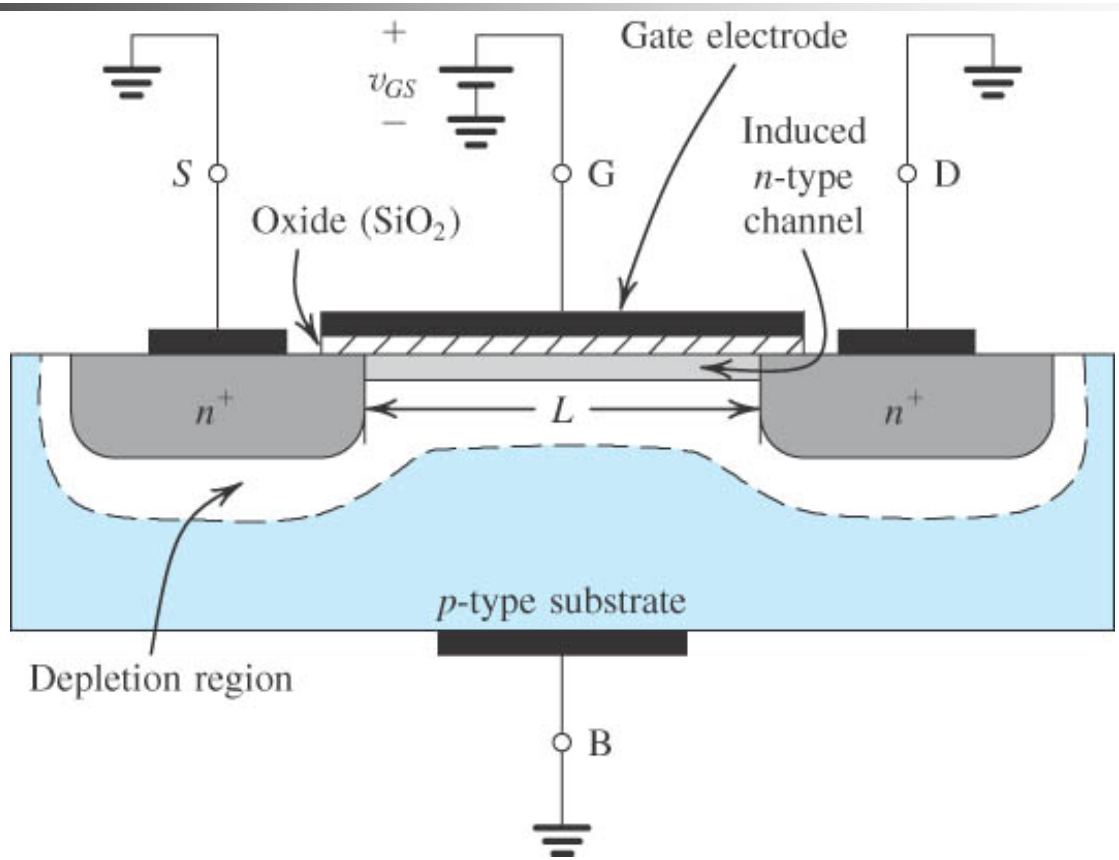
Structure of MOSFET





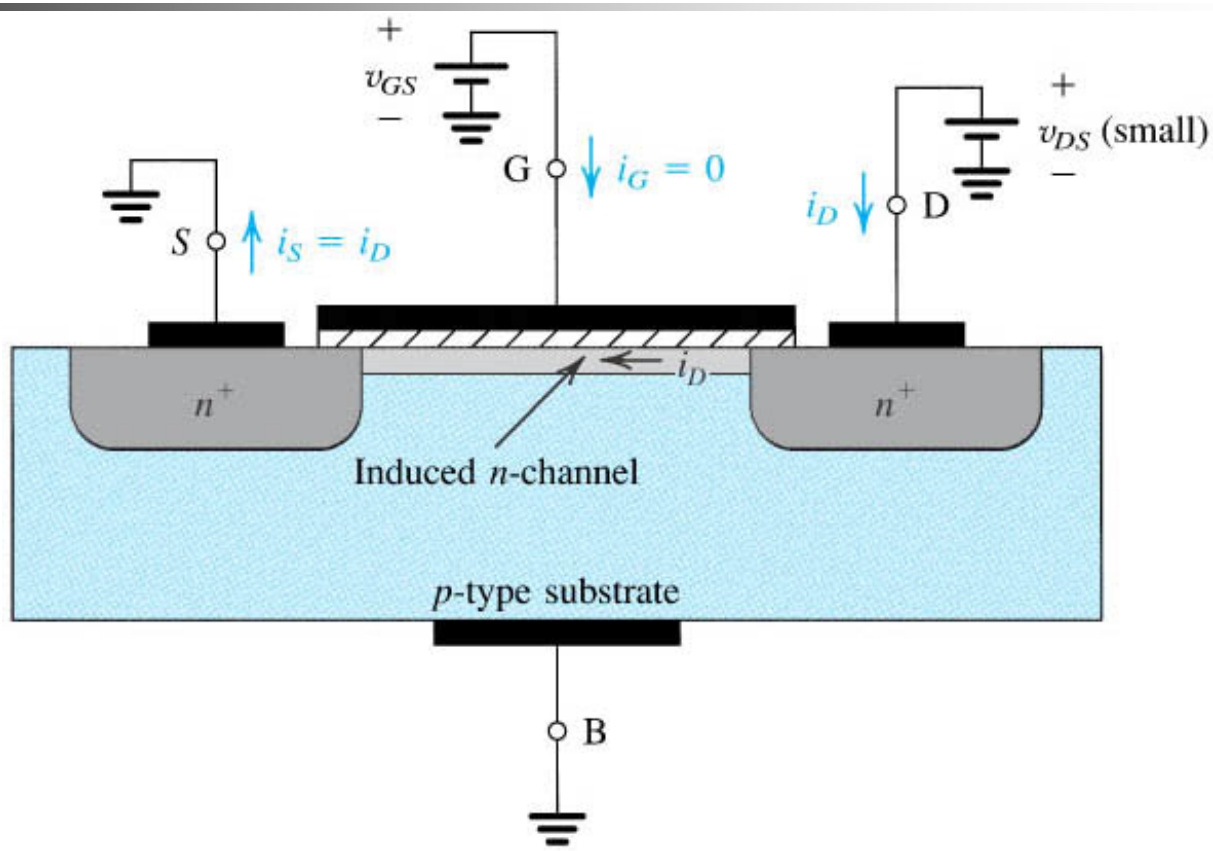
Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross-section. Typically *L* = 0.1 to 3 mm, *W* = 0.2 to 100 mm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

Mechanism of MOSFET



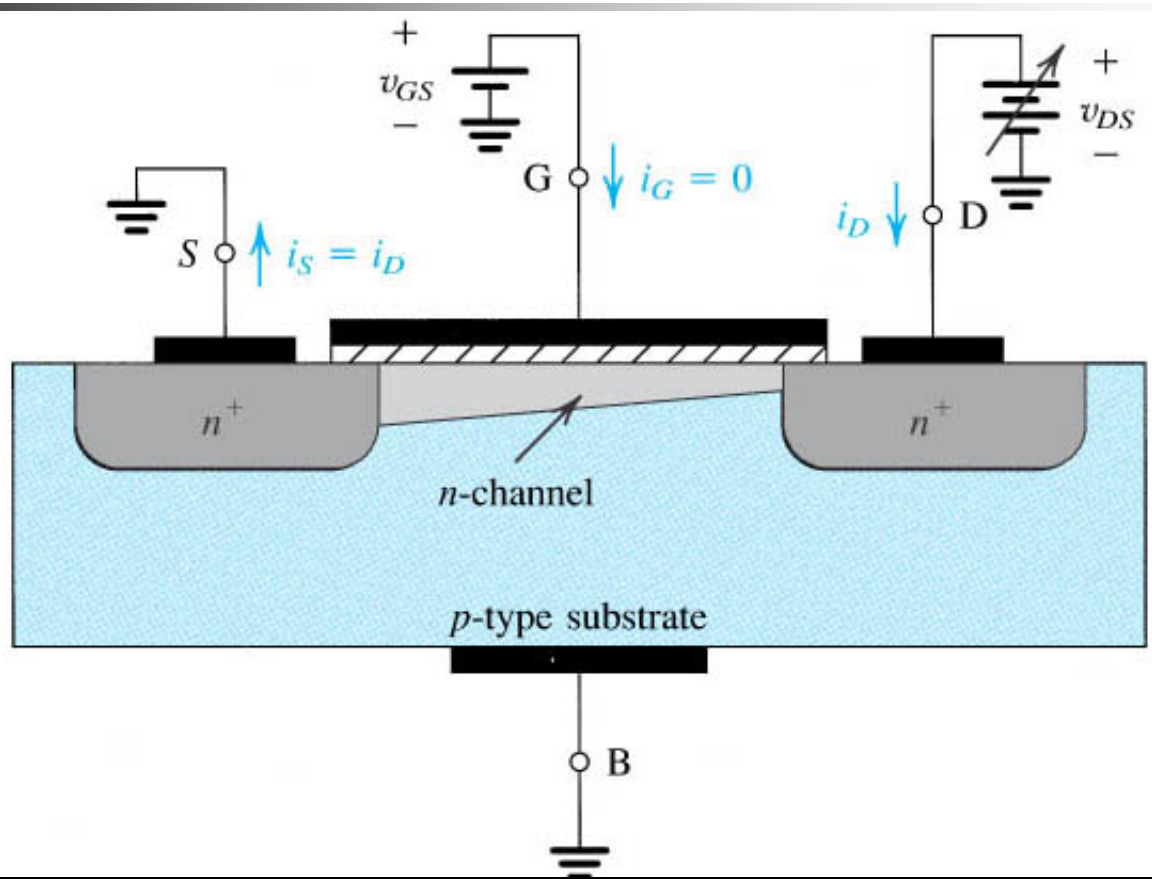
The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Mechanism of MOSFET



An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

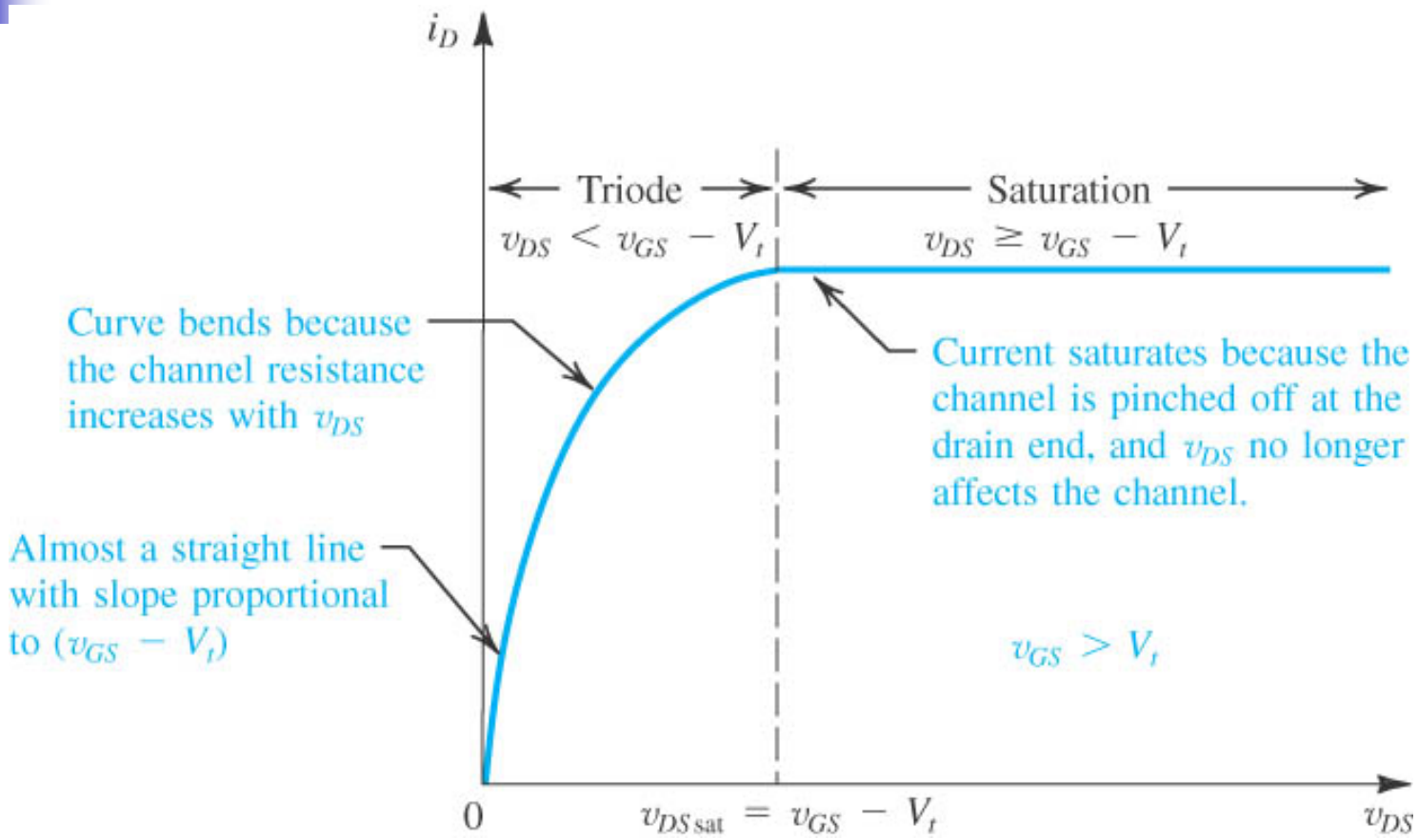
Mechanism of MOSFET



Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

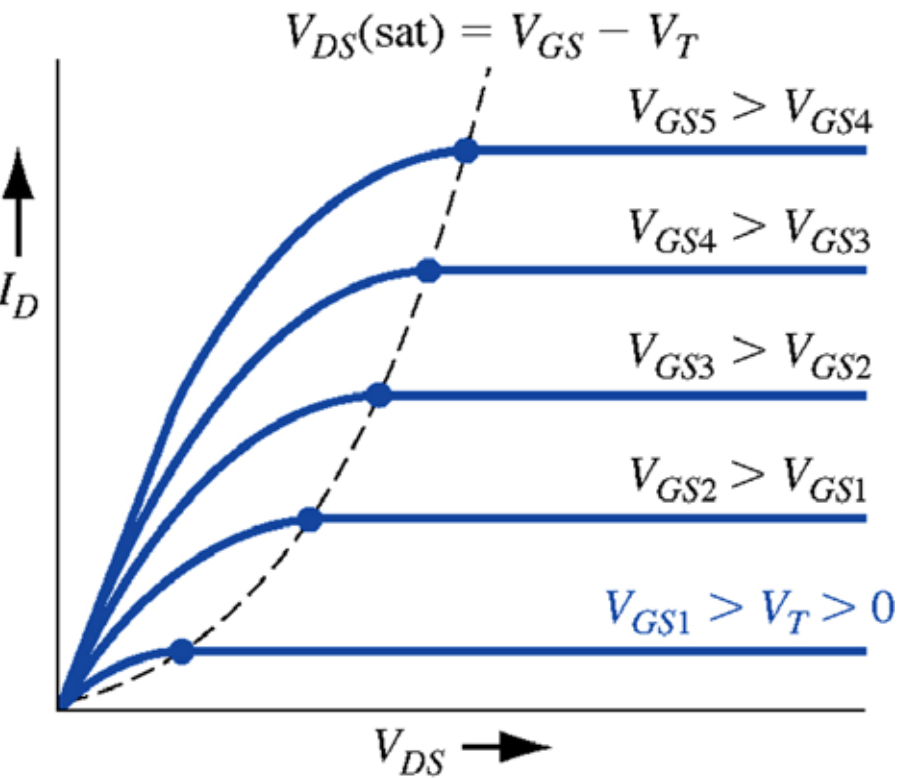
Mechanism of MOSFET

Threshold volatge $V_T \approx V_{FB} + 2\phi_{fn} + \frac{\sqrt{2 \in_S qN_A (2\phi_{fn} + V_{BS})}}{C_o}$; $\phi_{fn} = \frac{kT}{q} \ln(\frac{N_A}{n_i})$

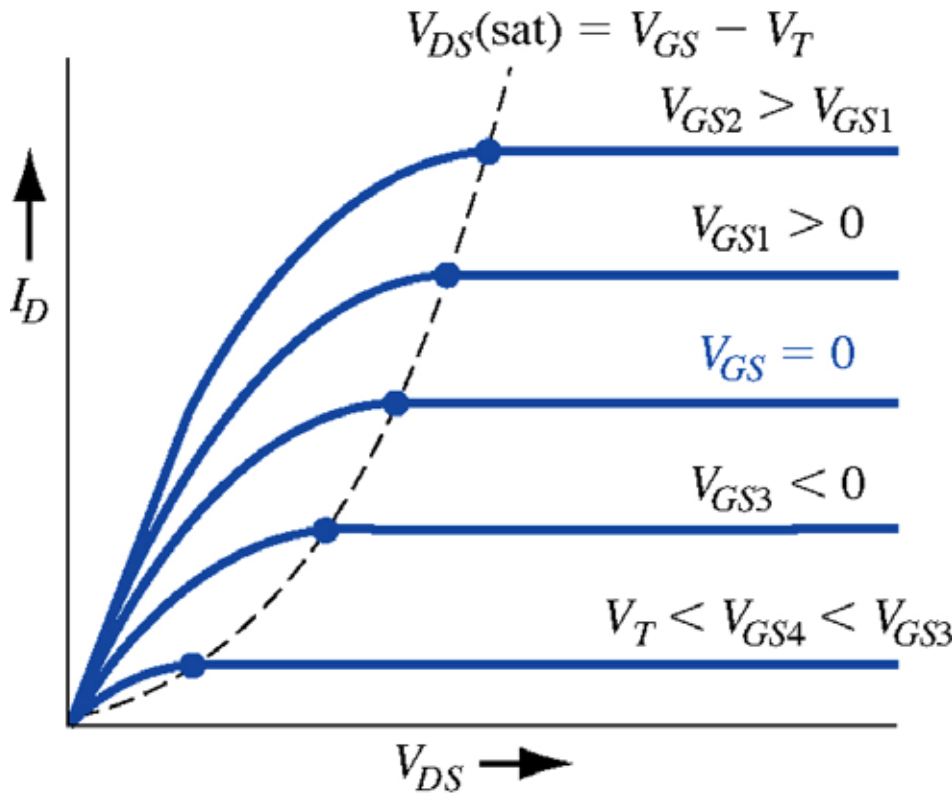


The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

Current-Voltage Relationship



Family of I_D versus V_{DS} curves for an n-channel enhancement-mode MOSFET



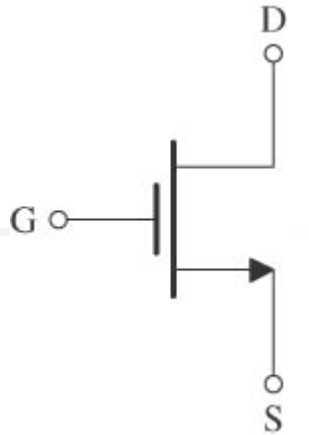
Family of I_D versus V_{DS} curves for an n-channel depletion-mode MOSFET

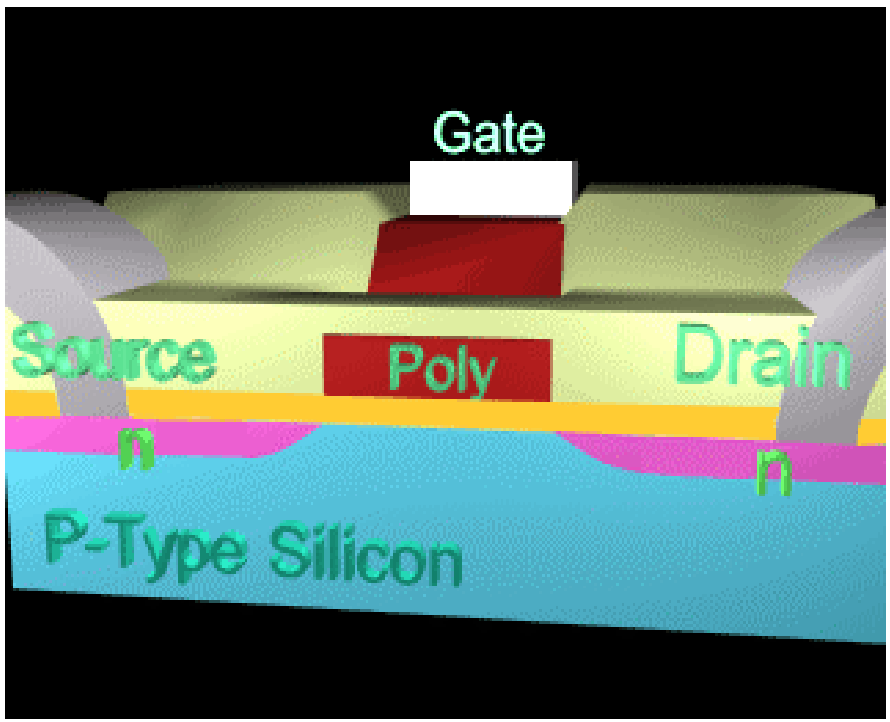
$$I_D = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad \text{(in non-saturation region)}$$

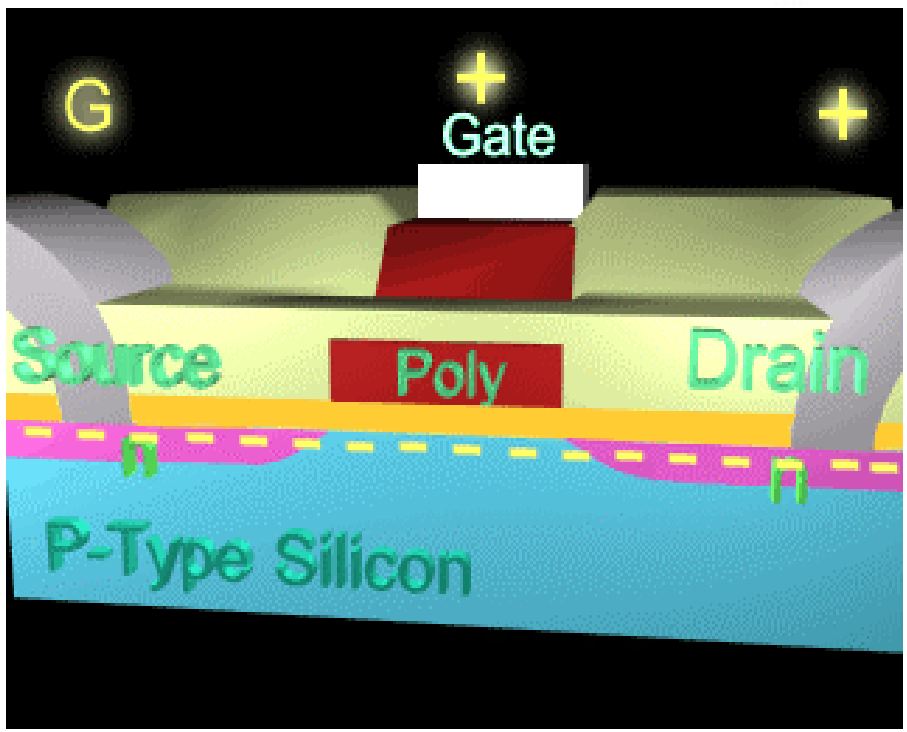
$$I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2 \quad \text{(in saturation region)}$$

N-channel Metal-Oxide-Semiconductor

- Gate – poly
- Source, Drain – n-type
- Substrate – p-type
- Carrier – electrons

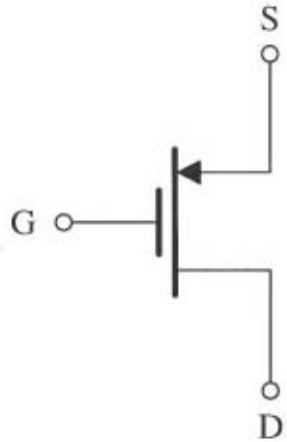


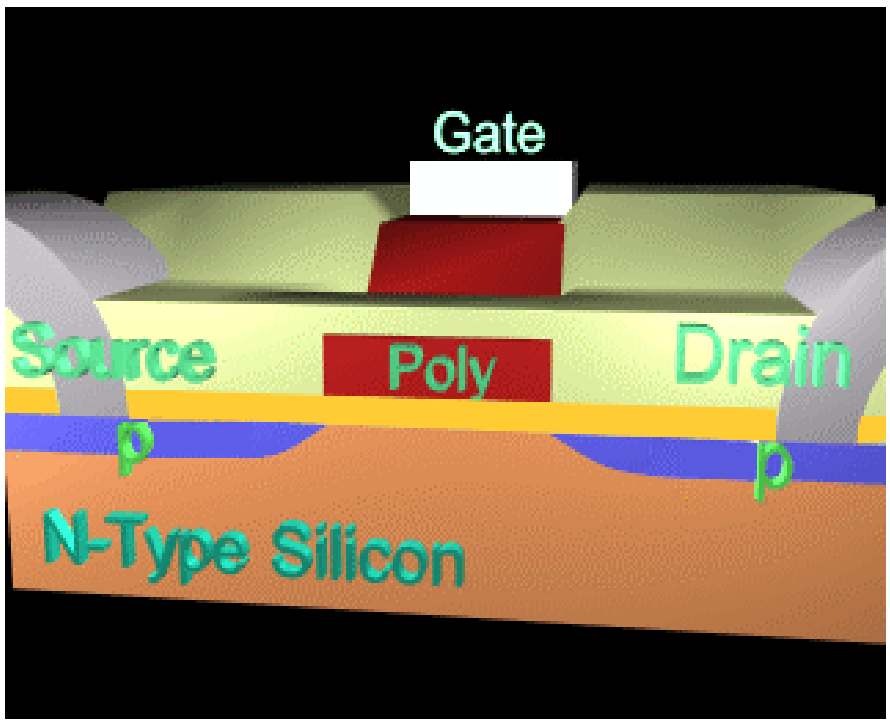


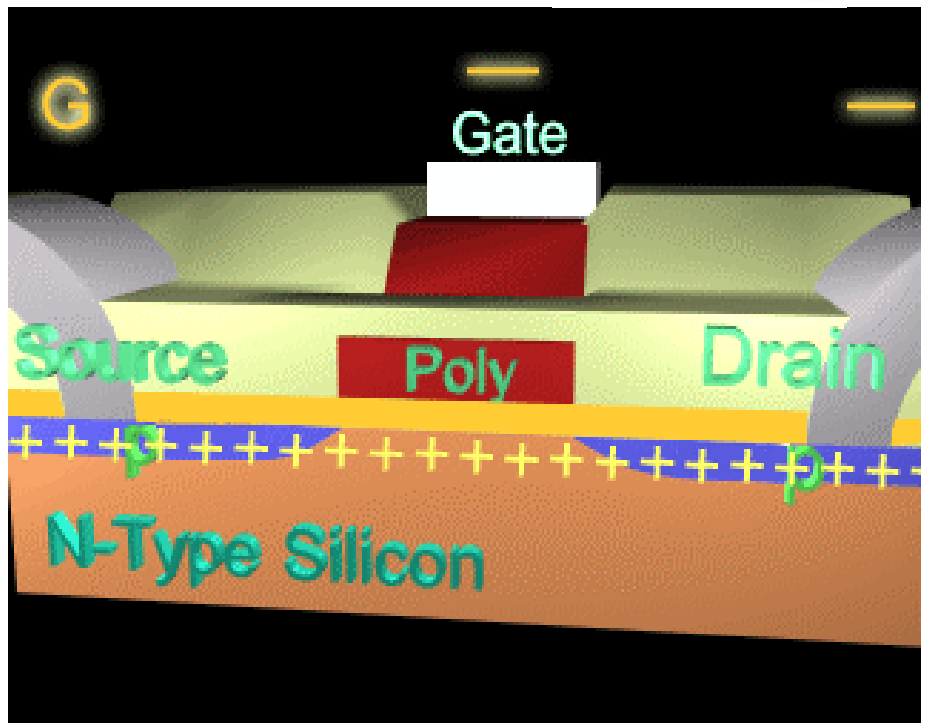


P-channel Metal-Oxide-Semiconductor

- Gate – poly
- Source, Drain – p-type
- Substrate – n-type
- Carrier – holes

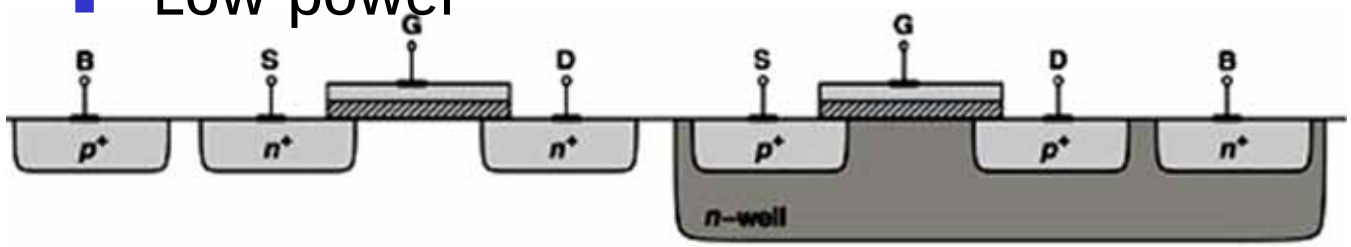




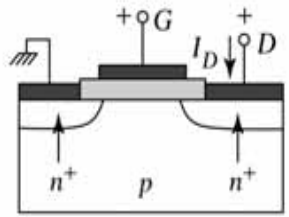
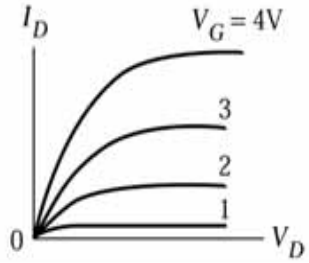
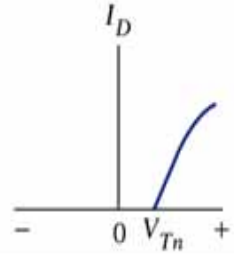
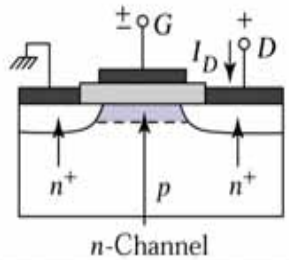
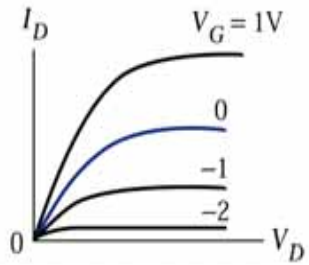
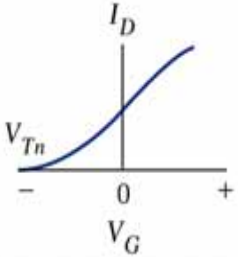
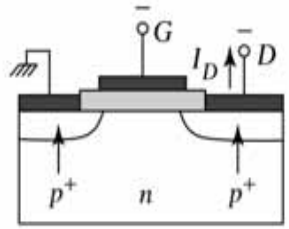
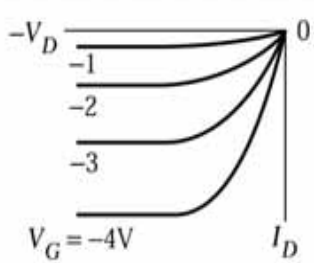
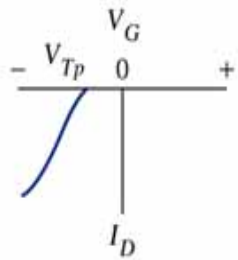
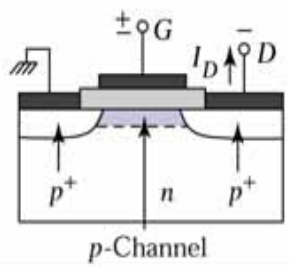
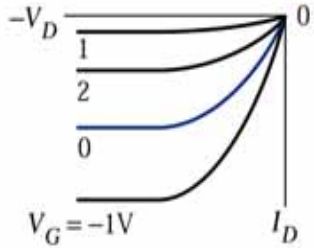
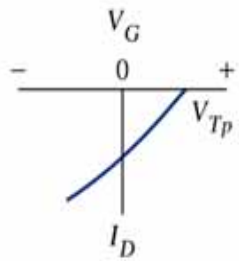


Complementary MOS (CMOS)

- NMOS + PMOS
  - Local substrate (n-well) for PMOS
- Advantage
  - High input impedance
  - Low power



Comparison of Enhancement and Depletion Mode MOSFETs

Type	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)			
n-Channel Depletion (Normally On)			
p-Channel Enhancement (Normally Off)			
p-Channel Depletion (Normally On)			

NMOS Fabrication Processes-(I)

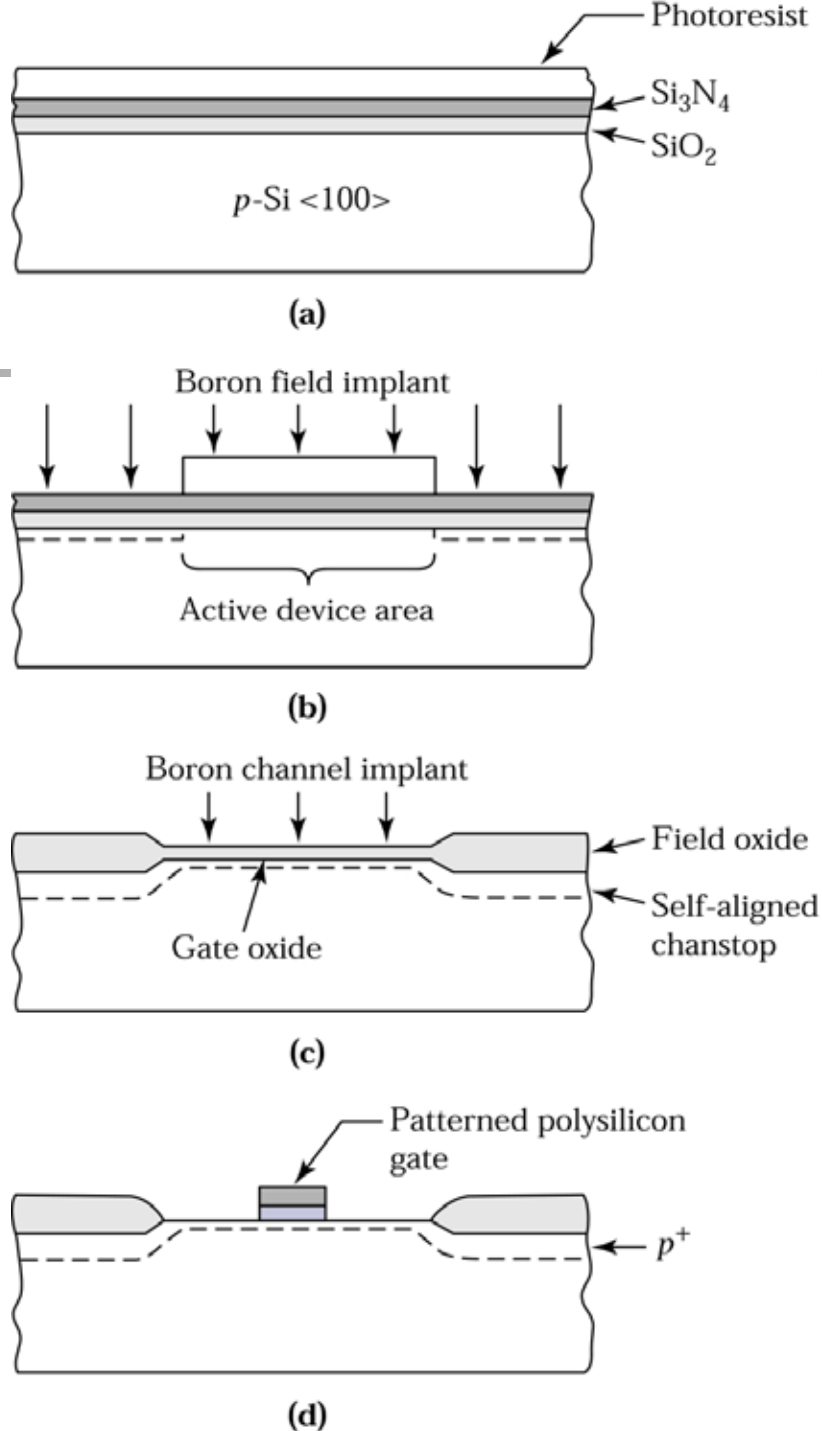
Cross-sectional view of NMOS fabrication sequence.

(a) Formation of SiO_2, Si_3N_4, and photoresist layer.

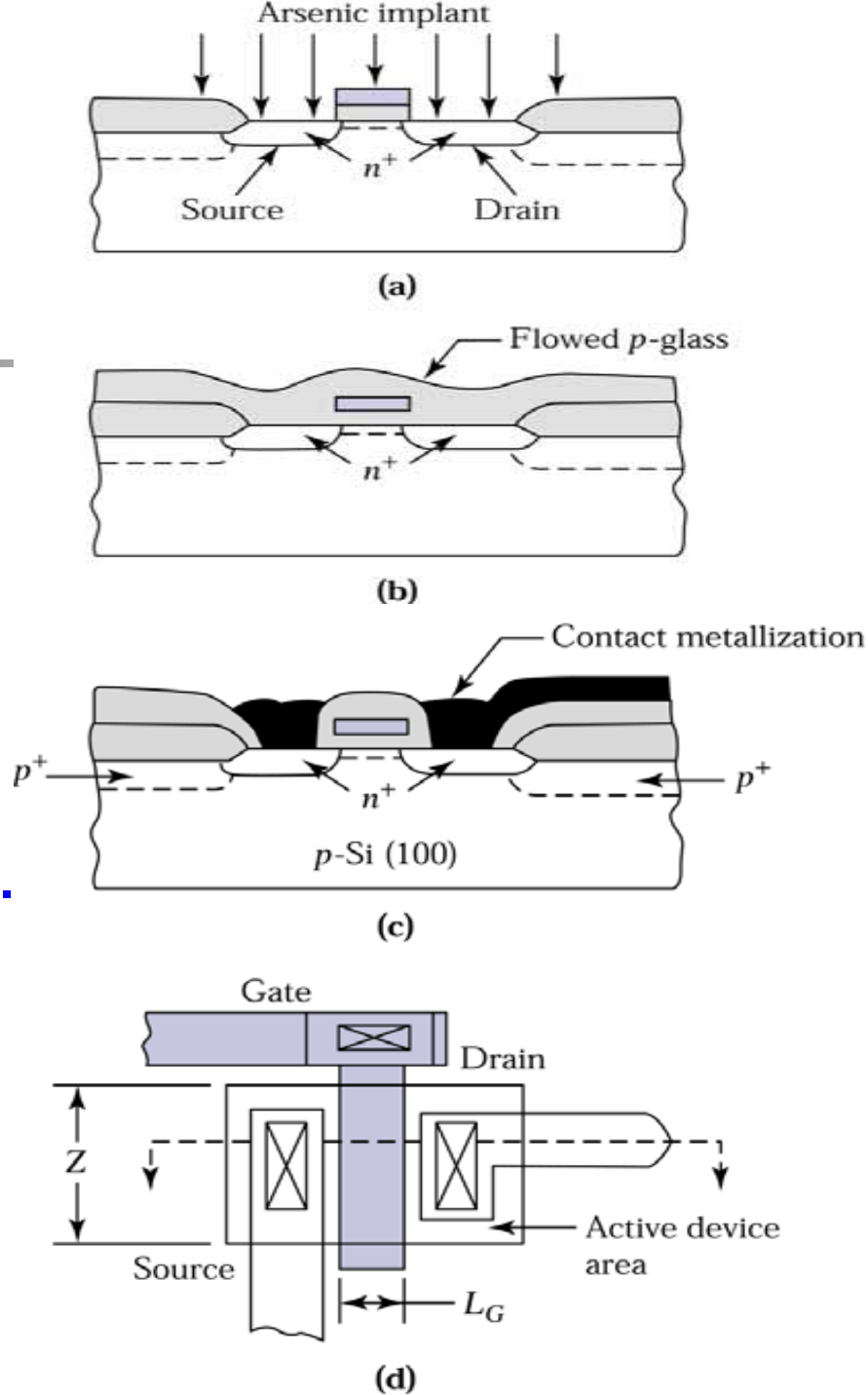
(b) Boron implant.

(c) Field oxide.

(d) Gate.



NMOS Fabrication Processes-(II)



NMOS fabrication sequence.

(a) Source and drain.

(b) P-glass deposition.

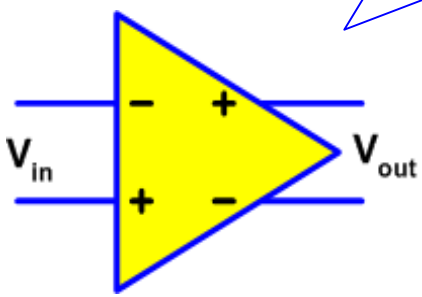
(c) Cross section of the MOSFET.

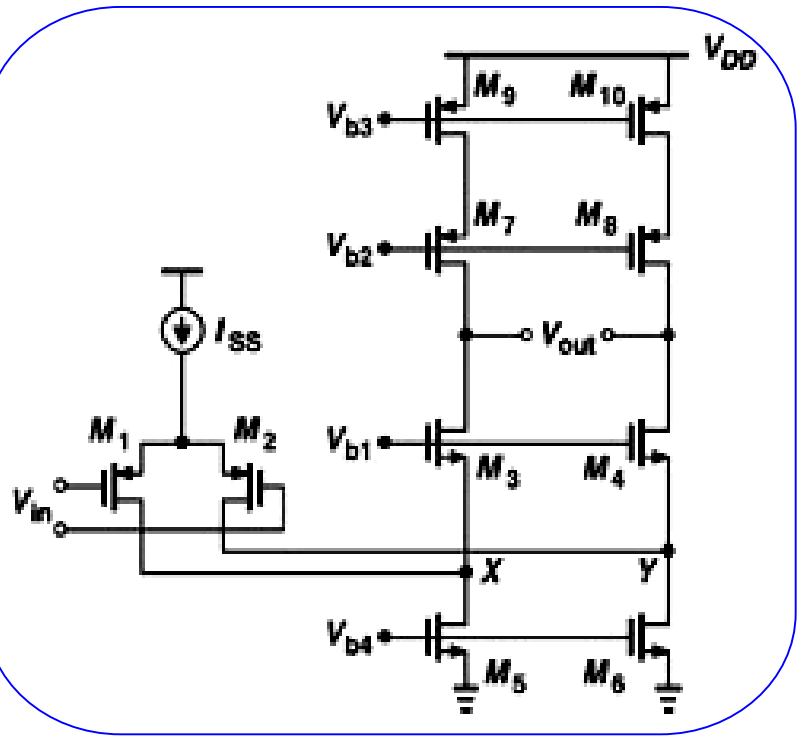
(d) Top view of the MOSFET.

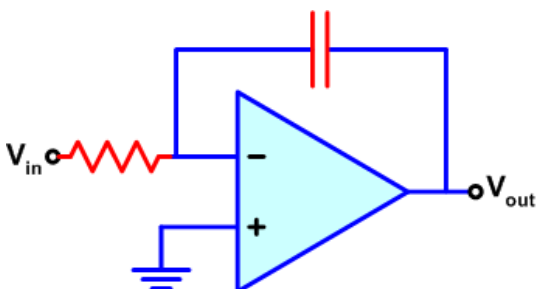
Applications of MOSFET

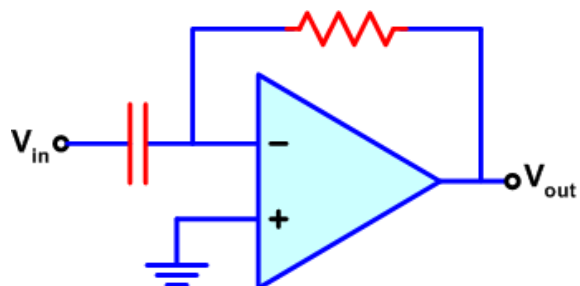
- **Analog Circuits**
  - Amplifiers, Adder, Integrator, Differentiator, …

$$\left|\frac{V_{out}}{V_{in}}\right| = A_0 \to \infty$$



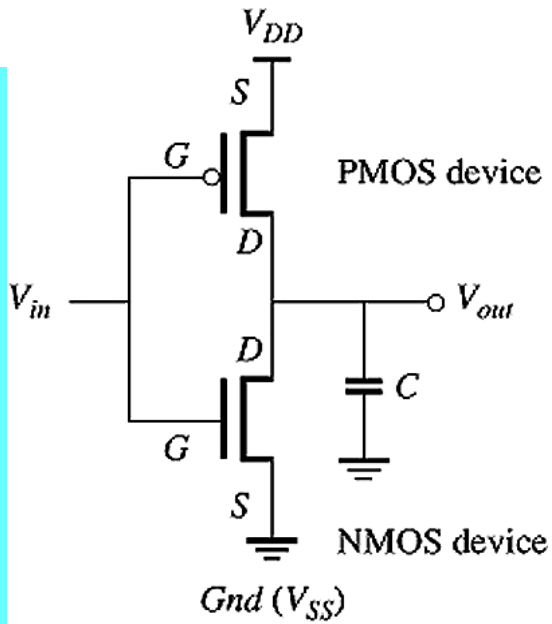






Applications of MOSFET

- **Digital Circuits**
  - PMOS device
    - Pull-up device connected to V_{DD}
    - Role : pull the output to high (1)
  - NMOS device
    - Pull-down device connected to ground
    - Role : pull the output to low (0)
  - Little power consumed in either high or low state
  - Boolean Algebra
    - Describe the functions of *logic gates*
      - *Inverter, NAND, NOR, XOR, ...*
  - Truth Table
    - The lists of Input/Output states



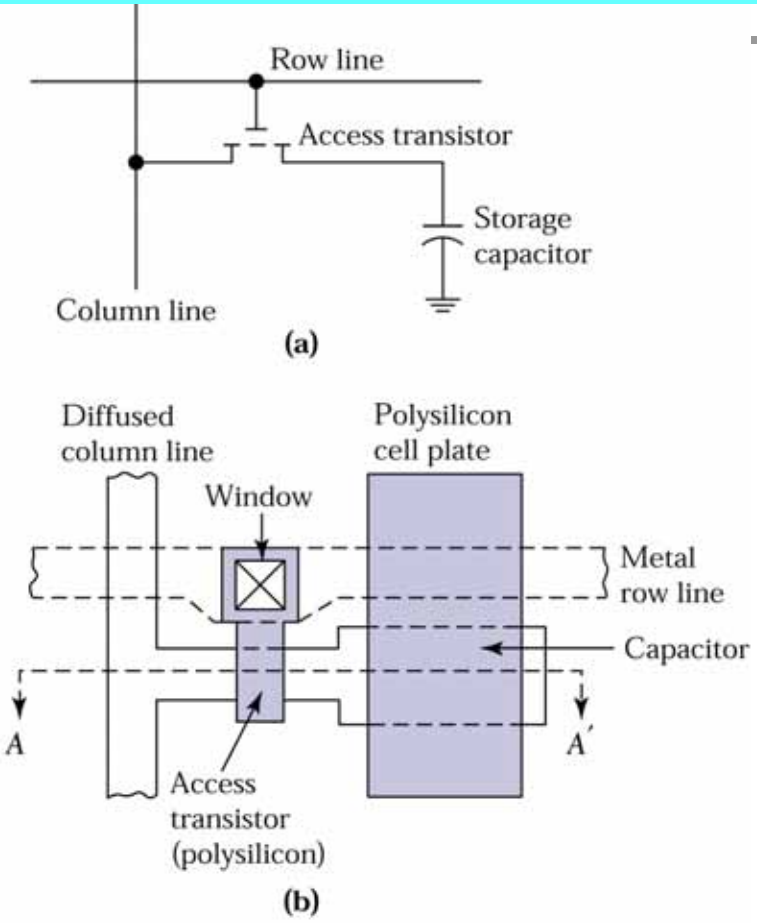
Inverter (INV)

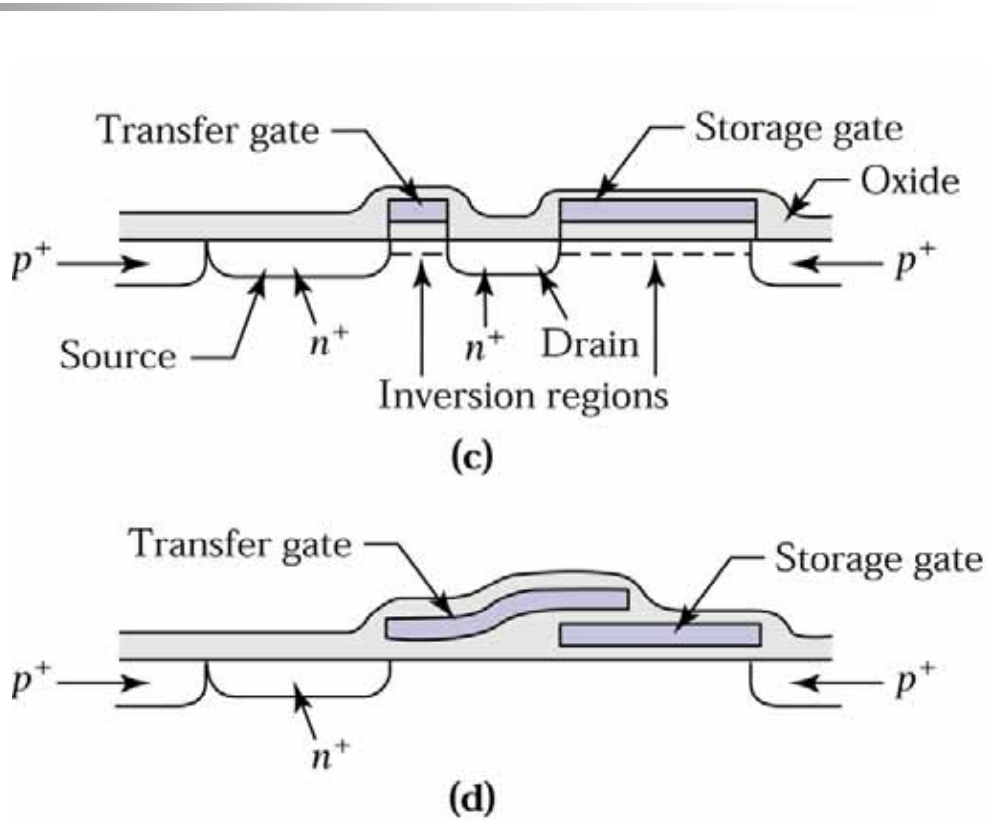
$$V_{out} = \overline{V_{in}}$$

V_{in}	V_{out}
0	1
1	0

SRAM : 1. can retain stored data indefinitely as long as the power supply is on.
2. One cell has 4 enhancement-mode and 2 depletion-mode MOSFETs.

DRAM : 1. The stored charge will be removed typical in a few nilliseconds mainly because of the leakage current of the capacitors; thus dynamic memories require periodic "refreshing" of the stored charge.
2. Has lower power consumption & cell area.

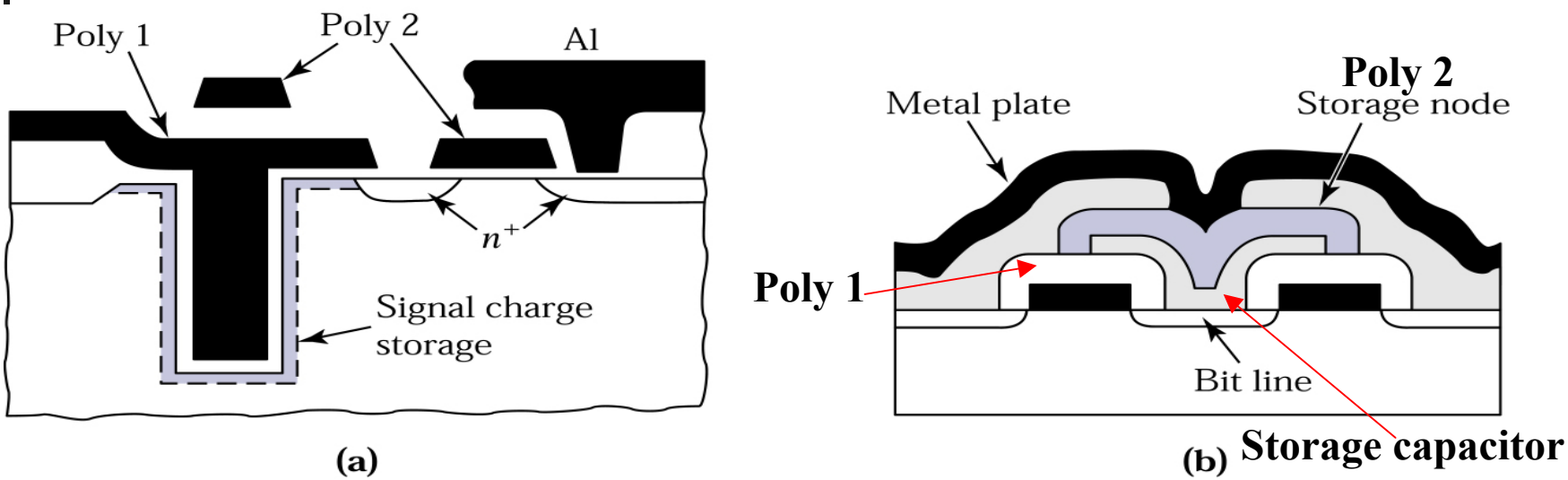




Single-transistor dynamic random access memory (DRAM) cell with a storage capacitor. (*a*) Circuit diagram. (*b*) Cell layout. (*c*) Cross section through *A-A'*. (*d*) Double-level polysilicon (*eliminate the drain region*)

Dynamic Random Access Memory (DRAM)

To meet the requirements of high-density DRAM, the DRAM structure extended to the third dimension with stacked or trench capacitors.



(a) DRAM with a trench cell structure

(b) DRAM with a single-layer stacked-capacitor cell.

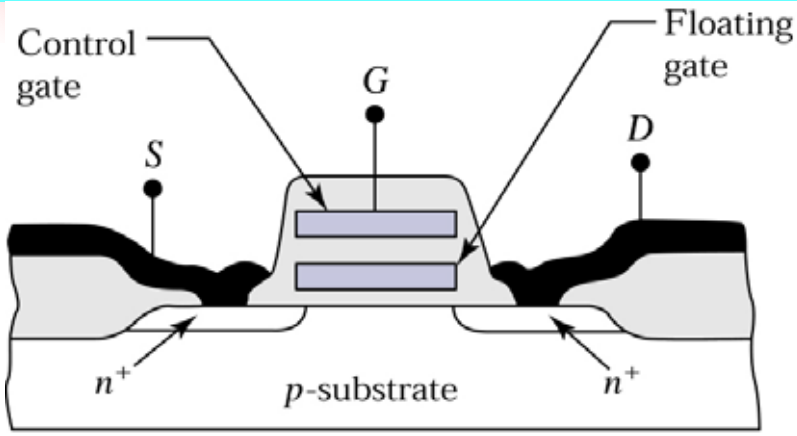
The capacitance of the cell could be increased by increasing the depth of the trench without increasing the surface area of silicon occupied by the cell. The main difficulties of making trench type cells are the etching of the deep trench, which needs a rounded bottom corner and the growth of a uniform thin dielectric film on trench wall

The stacked cell process is easier than the trench type process.

Nonvolatile Semiconductor Memory (NVSM)

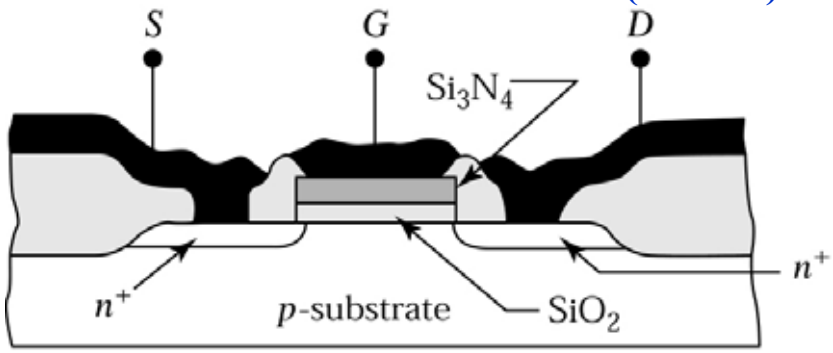
1. Applications : portable electronics systems (cellular phones & digital cameras) & IC card.

2. SRAM & DRAM are volatile memories, i.e. they lose their stored data when power is off

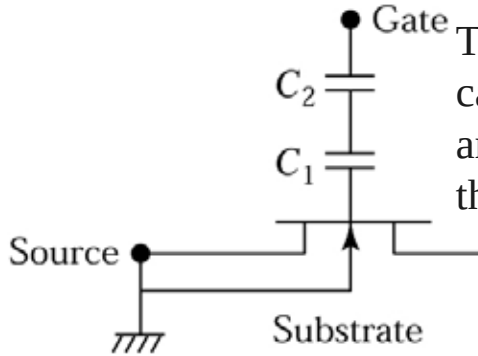


(a)

Metal-nitrid-oxide-semiconductor (MNOS)



(b)



(c)

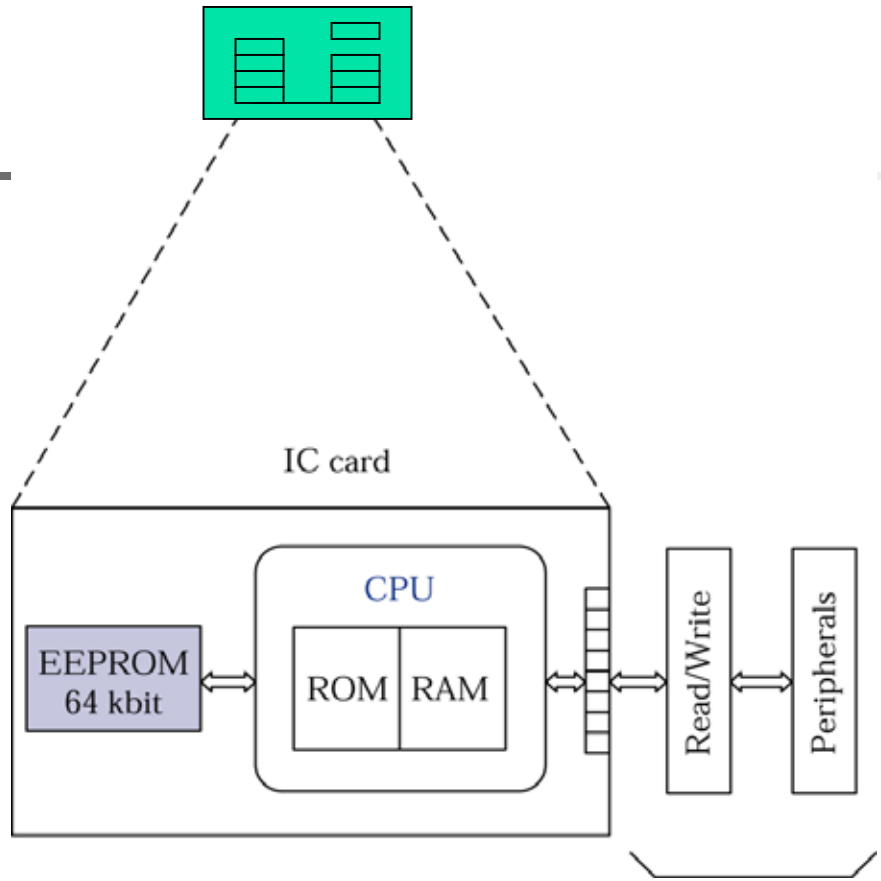
The charge stored in C_1 causes a shift in the V_{TH}, and the device remains at the higher V_{TH} sate (Logic 1)

When a large positive voltage is applied to the control gate, charge will be injected from the channel region through the gate oxide into the floating gate. When the applied voltage is removed, the injected charge can be stored in the floating gate for a long time. To remove this charge, a large negative voltage must be applied to the control gate, so that the charge will be injected back into the channel region.

Electrons can tunnel through the thin oxide layer(~2nm) and be captured by the traps at the oxide-nitride interface.

Nonvolatile memory devices. (*a*) Floating-gate, nonvolatile memory. (*b*) MNOS non-volatile memory. (*c*) Equivalent circuit of either type of nonvolatile memory.

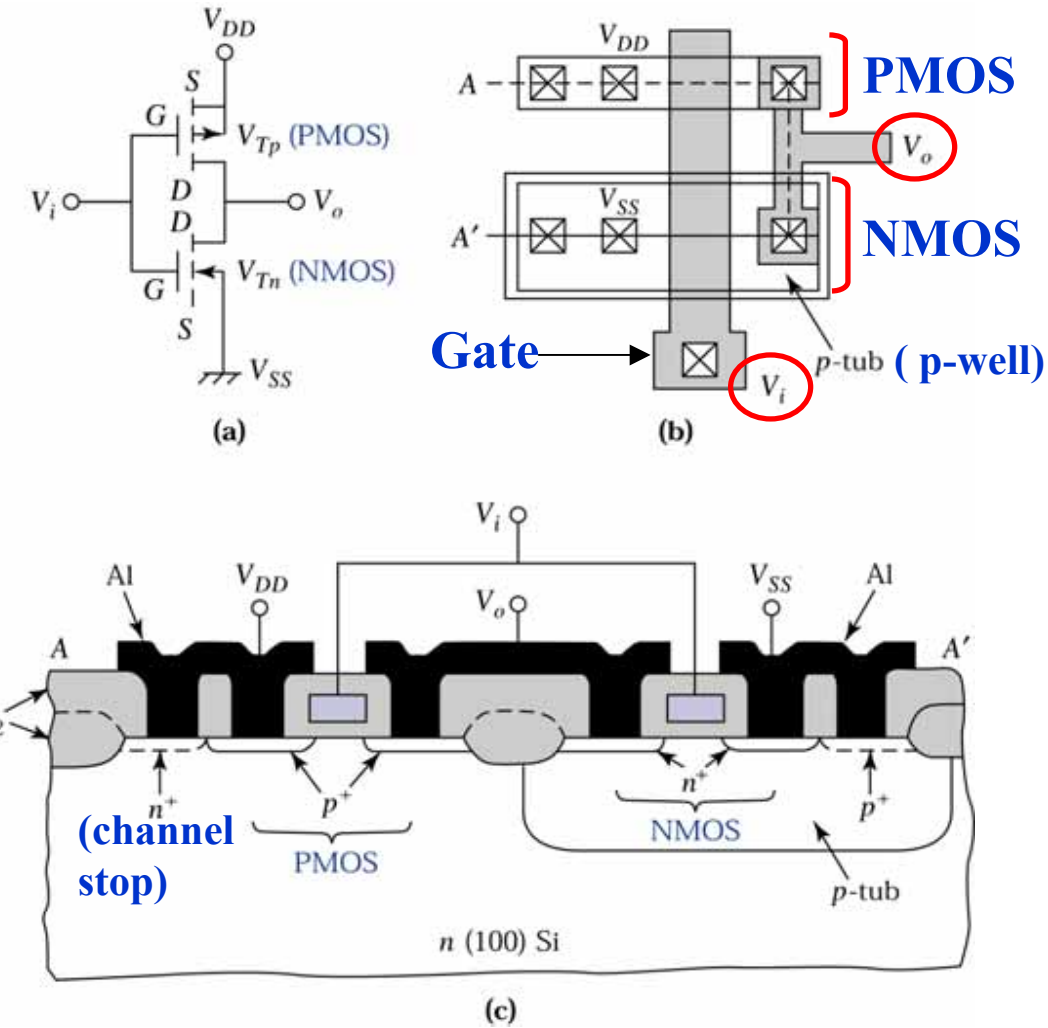
Integrated-Circuit (IC) Card



An integrated-circuit (IC) card. The data stored in the NVSM can be accessed through the bus of the central processing unit (CPU). There are several metal pads connecting to the read/write machine. (Photograph courtesy of Retone Information System Co., LTD.)

CMOS Technology
Complementary MOS (CMOS) Inverter

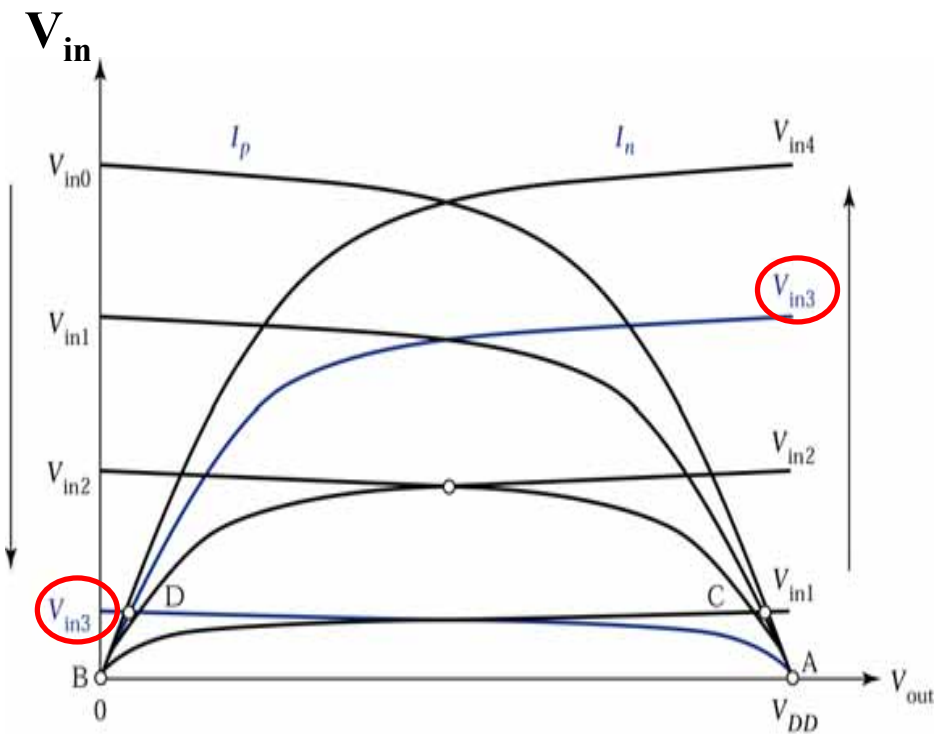
- Both devices are enhancement-mode (i.e. $V_{Tp} < 0$ & $V_{Tn} > 0$)
- When $V_i \geqq 0$, PMOS on & NMOS off
  - (a) $V_{GSp} \approx -V_{DD}$ *(more negative than V_{Tp})*
  - (b) $V_{GSn} < V_{Tp}$
  - hence $V_o \approx V_{DD}$ (Logic 1)
- When $V_i = V_{DD}$, PMOS off & NMOS on
  - (a) $V_{GSp} \approx 0$ & (b) $V_{GSn} < V_{Tp}$
  - Therefore, $V_o \approx 0$ (Logic 0)
- CMOS inverter has a unique feature : in either logic state, one device in the series path from V_{DD} to ground is nonconductive. The current that flows in either steady state is a small leakage current. Thus, the average power dissipation is small, on the order of nanowatts.



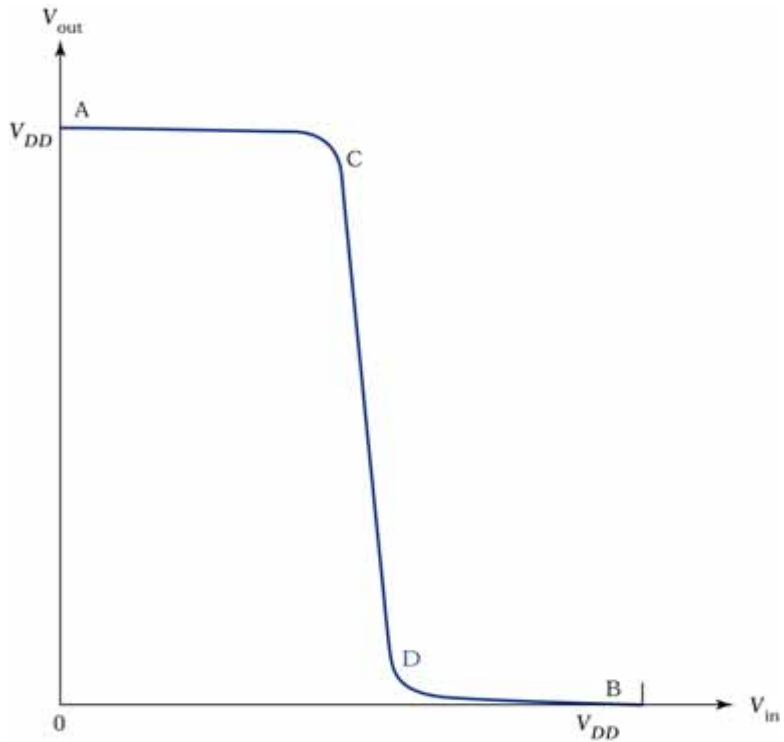
Feb. 2005

(*a*) Circuit diagram. (*b*) Circuit layout. (*c*) Cross section along dotted *A-A'* line of (*b*)

CMOS Technology
Complementary MOS (CMOS) Inverter



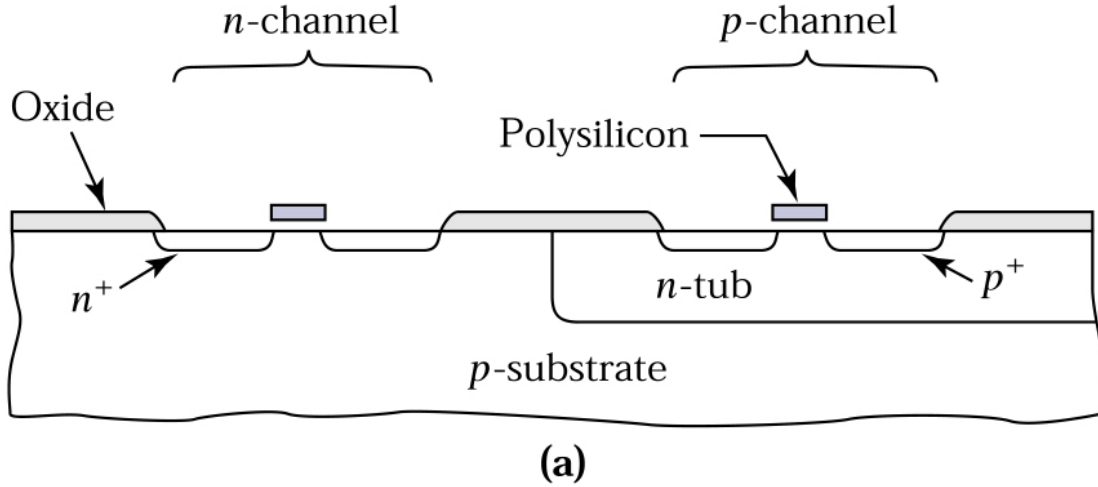
I_p and I_n as a function of V_{out}. The intercepts of I_p and I_n (circled) represent the steady-state operation points of the CMOS inverter.[11] The curves are labeled by the input voltages: 0 = $V_{in0} < V_{in1} < V_{in2} < V_{in3} < V_{in4} = V_{DD}$.



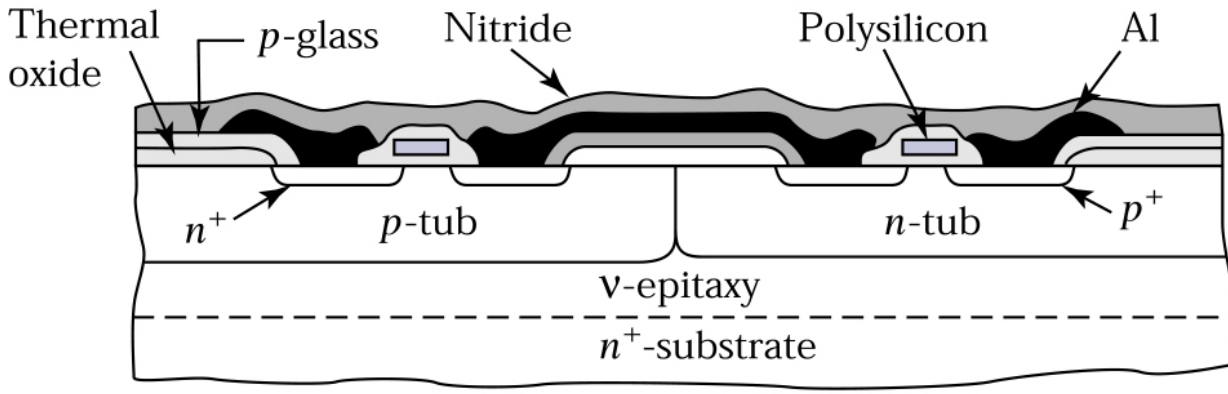
Transfer curve of a CMOS inverter. Points labeled A, B, C, and D correspond to those points labeled in left figure

CMOS Technology Various CMOS Structure

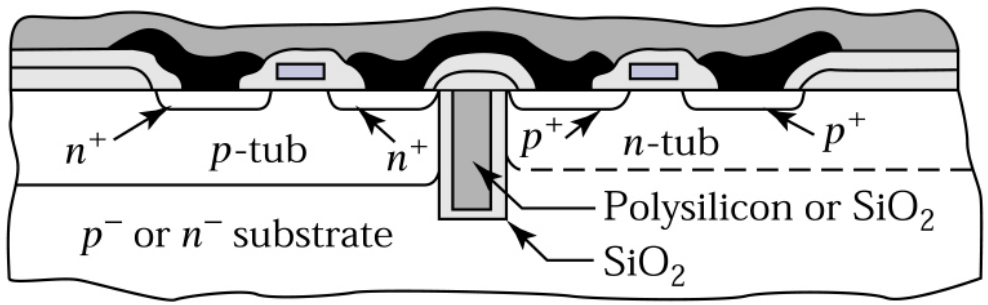
(a) *n*-tub.
(b) Twin tub
(c) Refilled trench



(a)



(b)

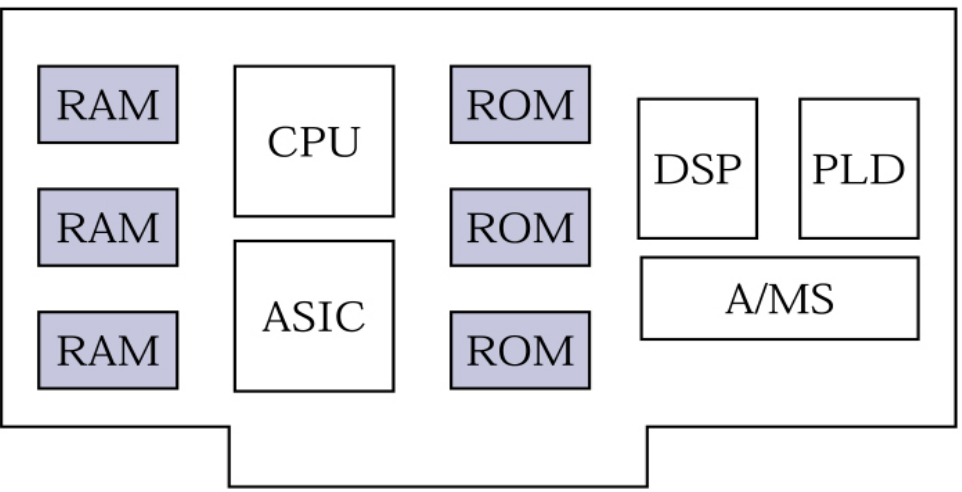


(c)

Feb. 2005
中山電機系　黃義佑

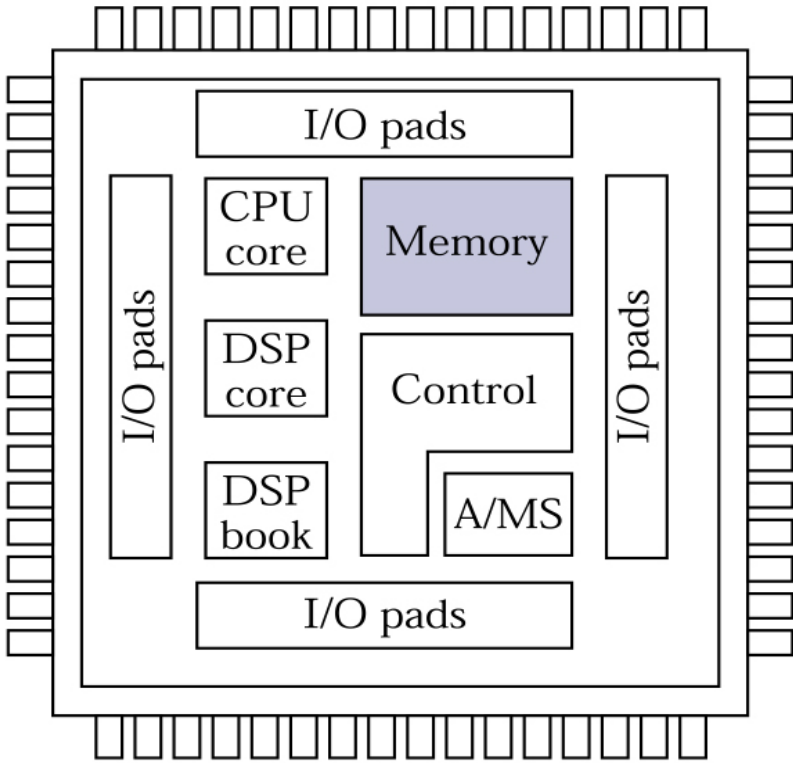
System Level : System-On-a-Chip (SOC)

A/MS = analog/mixed signal
ASIC = application-specific IC
CPU = central processing unit
PLD = programmable logic device



Components : 11 chips

Board components



Virtual components

System-On-a-Chip (SOC) of a Conventional Personal Computer Mother-board

Difficulty of Design: different companies & different design tools, it is difficult to integrate

Difficulty of Fabrication: DRAM process are significant different to logic IC (e.g. CPU)