Chapter 2 :
Semiconductor Materials & Devices (I)

Reference

1. **SemiconductorManufacturing Technology*: Michael Quirk and Julian Serda (2001)***
2. 國家矽導計畫-教育部晶片法商學程編定教材
3. **ULSI Technology *: C. Y. Chang, S. M. Sze (1996)***
4. **Semiconductor Physics and Devices- Basic Principles (3/e) *: Donald A. Neamen (2003)***
5. **Semiconductor Devices *- Physics and Technology* (2/e) *: S. M. Sze (2002)***

- 何謂半導體？(基本半導體特性)
- 半導體之分類
- 半導體材料之結構
- 一般晶格所常用之術語
- 半導體材料之成長

何謂半導體？

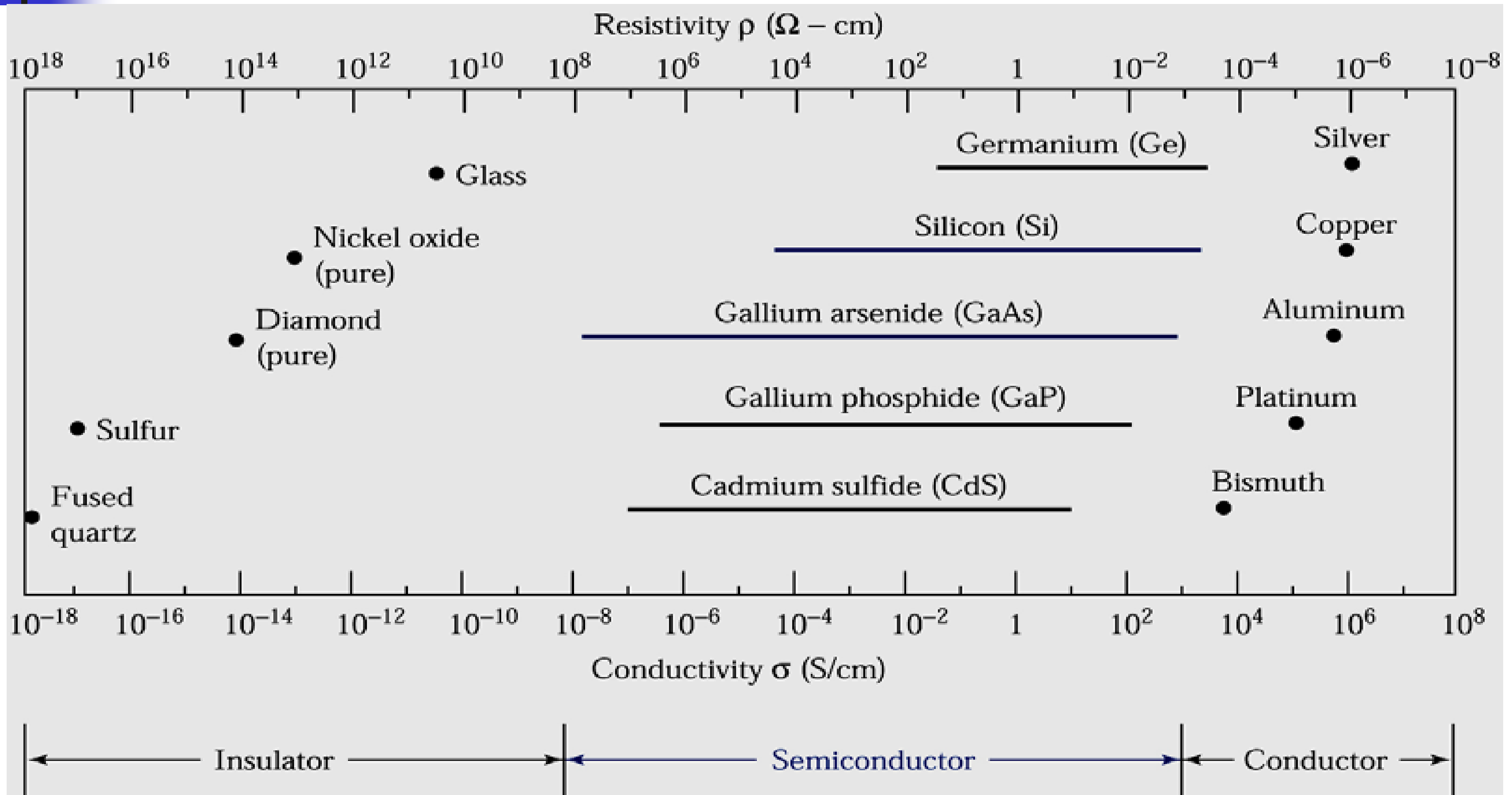
•以通俗的字眼來說便是一種材料它的導電度介於金屬與非金屬之間: $10^4 \sim 10^{-10}$ $(\Omega cm)^{-1}$。

•以專業的眼光來看便是該材料的電阻值可藉由摻入雜質(impurity)的種類、數量來調整。

•雜質種類的不同將可以決定載子(carrier)的型態。當有特定區域適合這兩種型態的載子相互結合時，電子元件的種種特性便接踵而來。

What is Semiconductor

- Conductivity between conductor and insulator



與半導體相關之週期元素
Element Semiconductors

Table 1 Portion of the Periodic Table Related to Semiconductors

Period	Column II	III	IV	V	VI
2		B Boron	C Carbon	N Nitrogen	
3	Mg Magnesium	Al Aluminur	Si Silicon	P Phosphorus	S Sulfur
4	Zn Zinc	Ga Gallium	Ge Germanium	As Arsenic	Se Selenium
5	Cd Cadmium	In Indium	Sn Tin	Sb Antimon;	Te Tellurium
6	Hg Mercury		Pb Lead		

Why Silicon Can Dominate the IC Industry ?

Silicon devices exhibit better properties at room temperature, and high-quality silicon dioxide can be grown thermally. There is also an economic consideration. Device-grade silicon costs much less than any other semiconductor material.

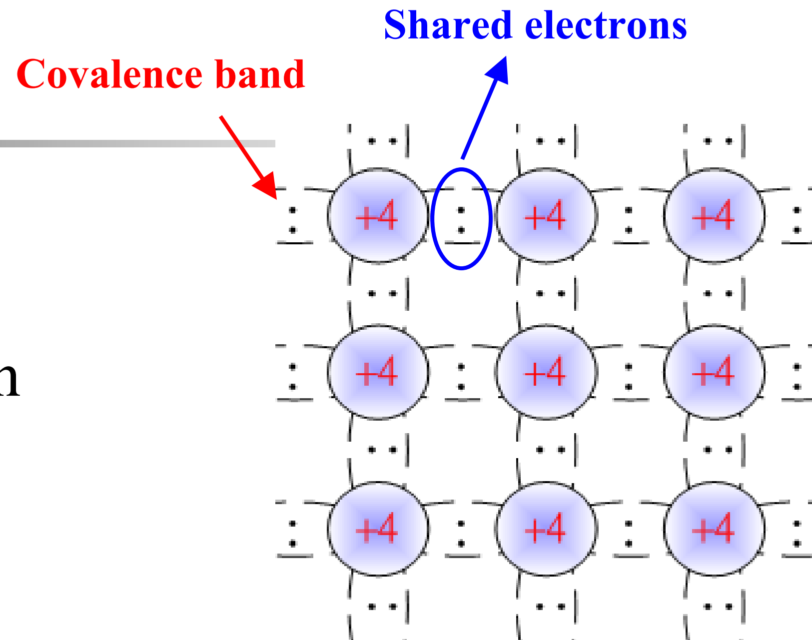
半導體分類

- 基本上以週期表的第四族為基準點，其共通特性是每一原子平均有四個價電子
- 事實上近年來材料的演進極為快速，凡是與電子元件工業相關連的材料都被統稱電子材料，而半導體材料的定義逐漸廣義化，凡是可以產生正負型載子的材料都可稱之半導體。
- 傳統上半導體材料依舊落於無機材料，近年來有機材料正被重視當中。

Table 2 Element and Compound Semiconductors

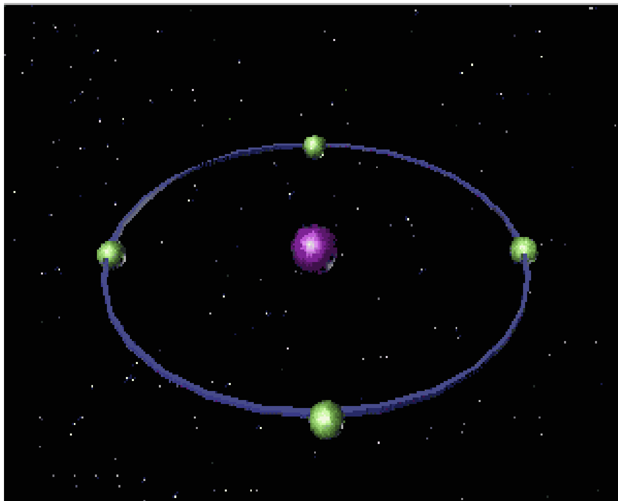
Element	IV–IV Compounds	III–V Compounds	II–VI Compounds	IV–VI Compounds
Si	SiC	AlAs	CdS	PbS
Ge		AlSb	CdSe	PbTe
		BN	CdTe	
		GaAs	ZnS	
		GaP	ZnSe	
		GaSb	ZnTe	
		InAs		
		InP		
		InSb		

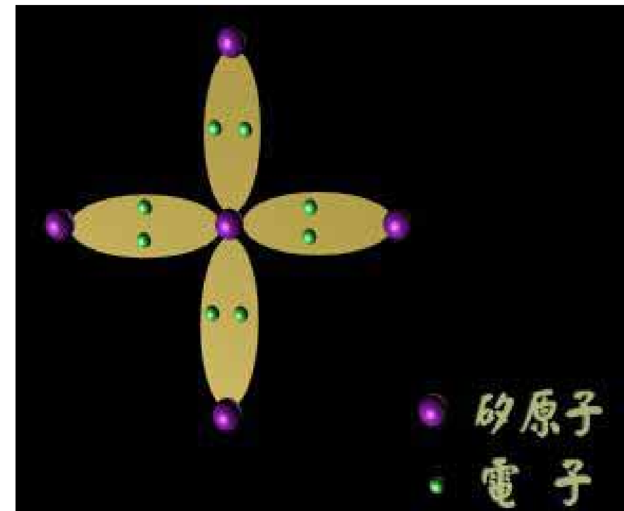
Silicon Structure



Silicon Atom

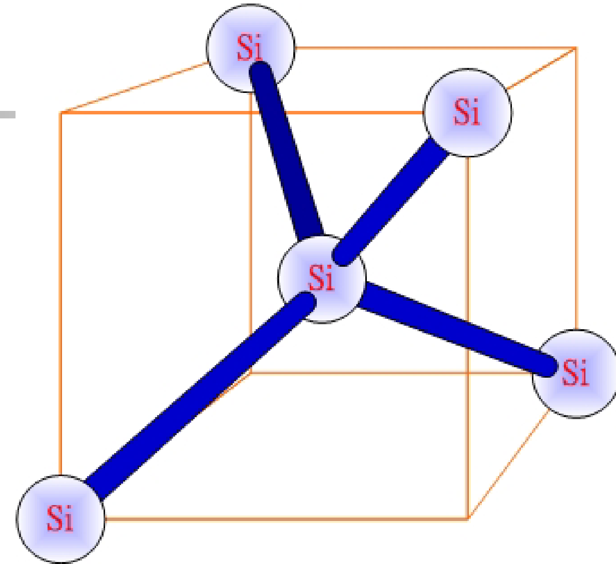
- Quadrivalent element
  - Four valence electron
- Atomic number = 14
  - 4 valence electron
- Covalent bond

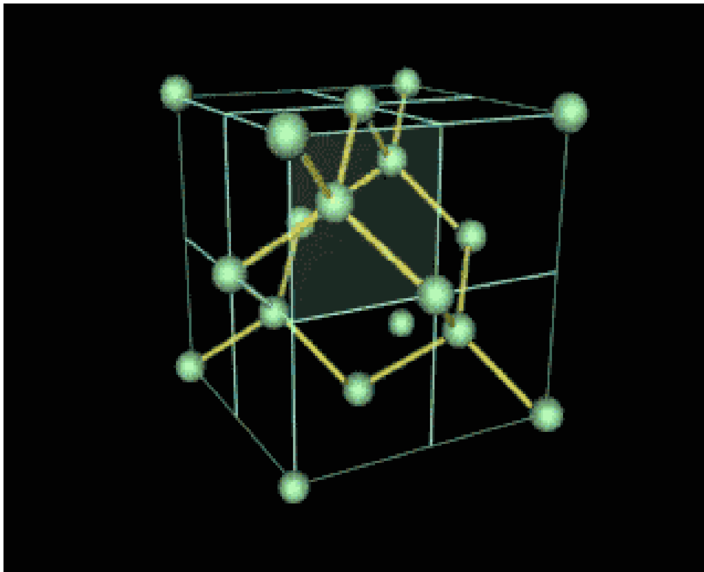


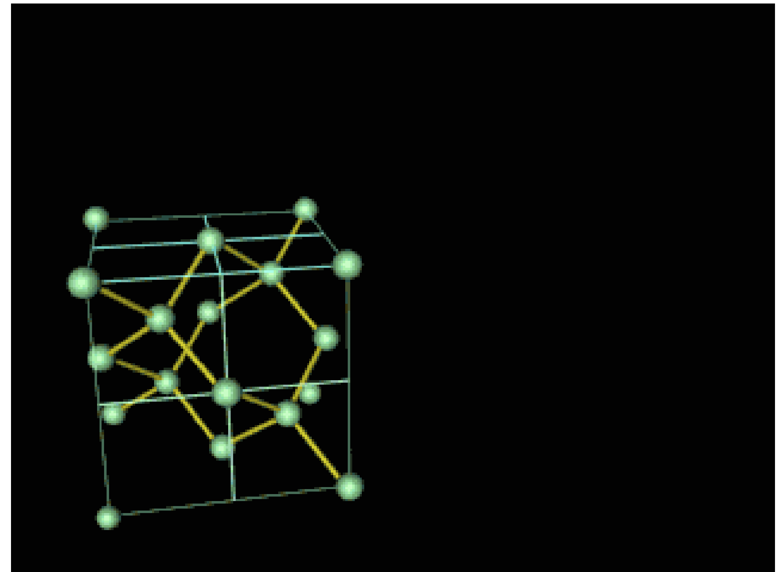


Silicon Structure

Diamond Structure

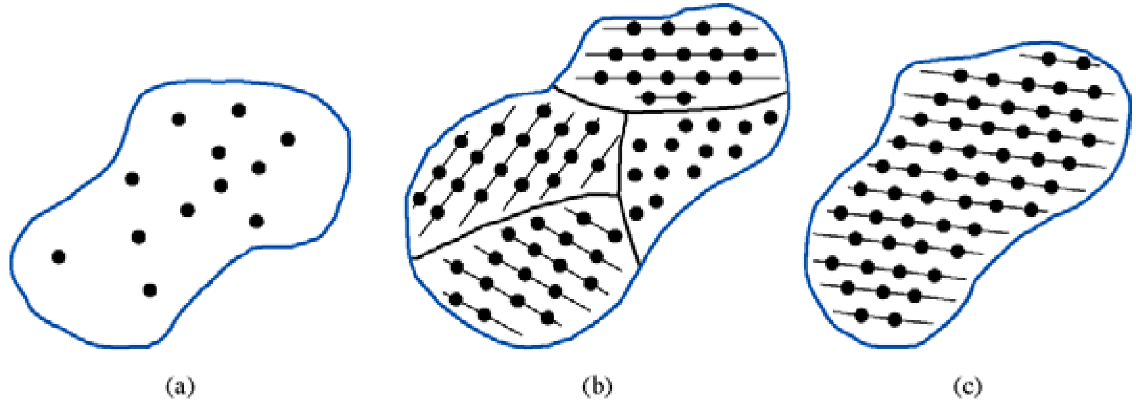






半導體材料結構

一般材料結構可區分為非晶系，多晶系以及單晶系。其重大的區別在於原子排列規則性持續的程度大小而定



Schematics of three general types of crystals:(a) amorphous, (b) polycrystalline, (c) single crystal.

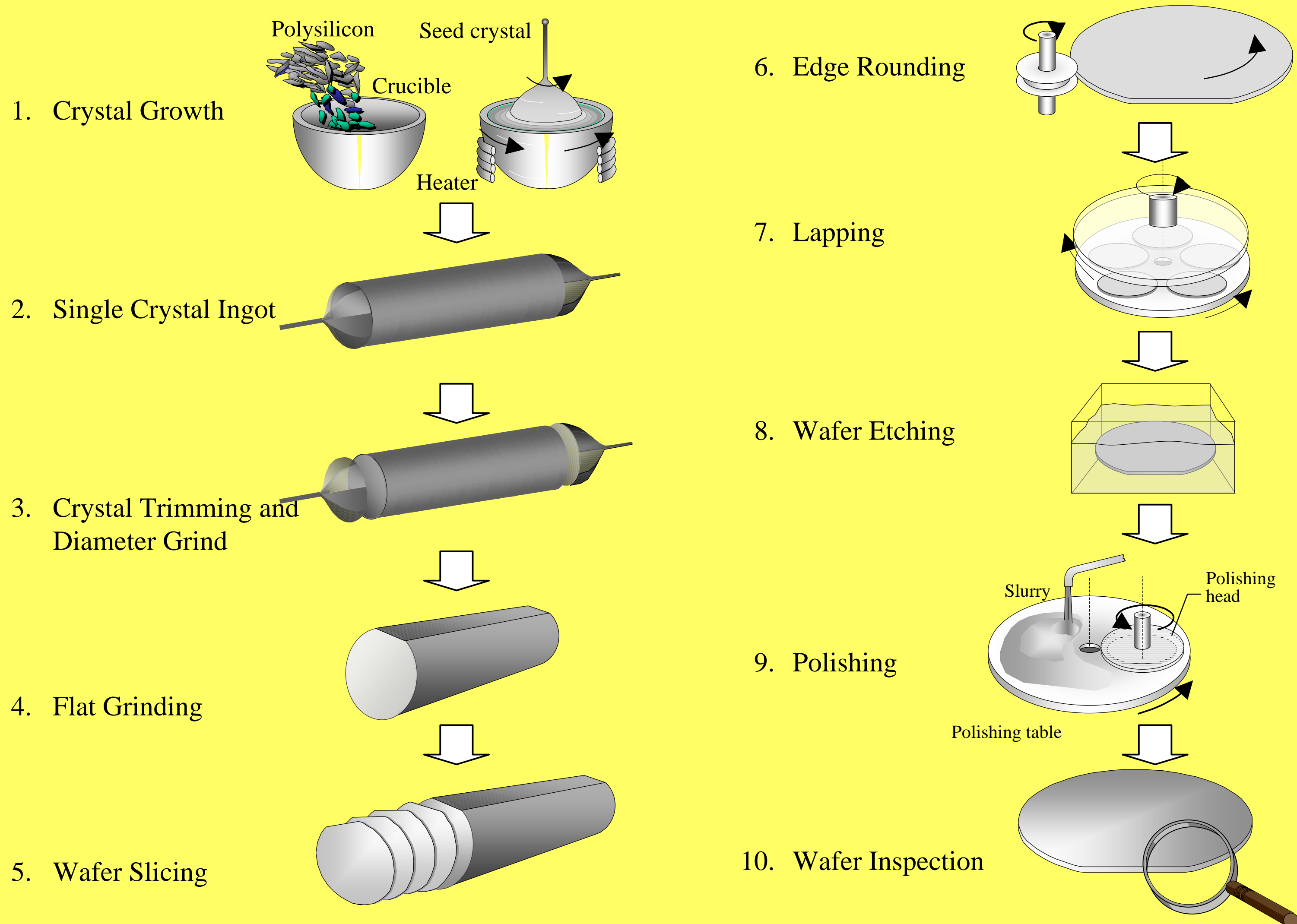
Amorphous materials have order only within a few atomic or molecular dimensions.

Polycrystalline materials have a high degree of order over many atomic or molecular dimensions. These ordered regions, or single-crystal regions, vary in size and orientation with respect to one another. The single-crystal regions are called ***grains*** and are separated from one another by ***grain boundaries***.

Single-crystal materials, ideally, have a high degree of order, or regular geometric periodicity, throughout the entire volume of the material. The advantage of a single-crystal material is that, in general, its electrical properties are superior to those of a non-single crystal material, since **grain boundaries tend to degrade the electrical characteristics**

.在半導體元件應用上，該三種型態結構都有其應用的價值。唯獨當元件是用來作為主動元件時，則該半導體必須是單晶型態。

Preparation of Single Crystal Silicon Wafers



General Characteristics of Silicon Wafer

Diameter: 10~30cm, 20cm(8-inch)

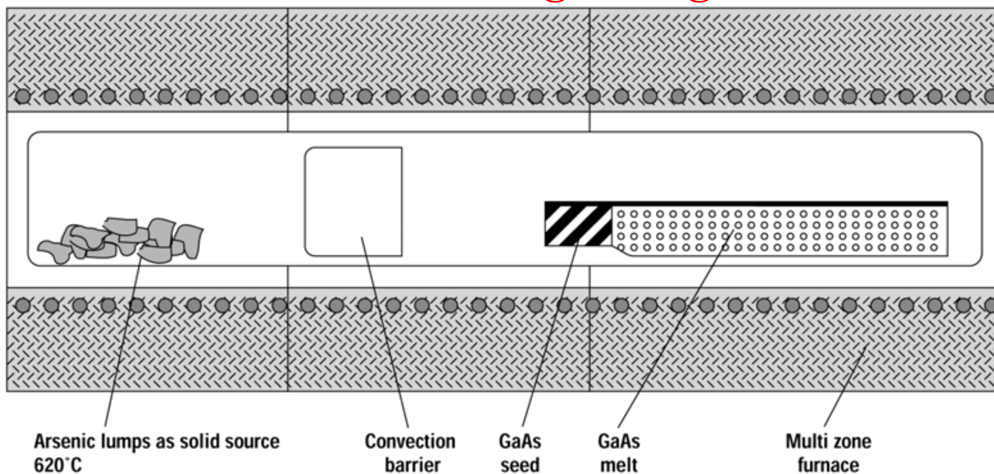
Thickness: 400~600μm

Resistivity: 0.05~0.1Ωcm

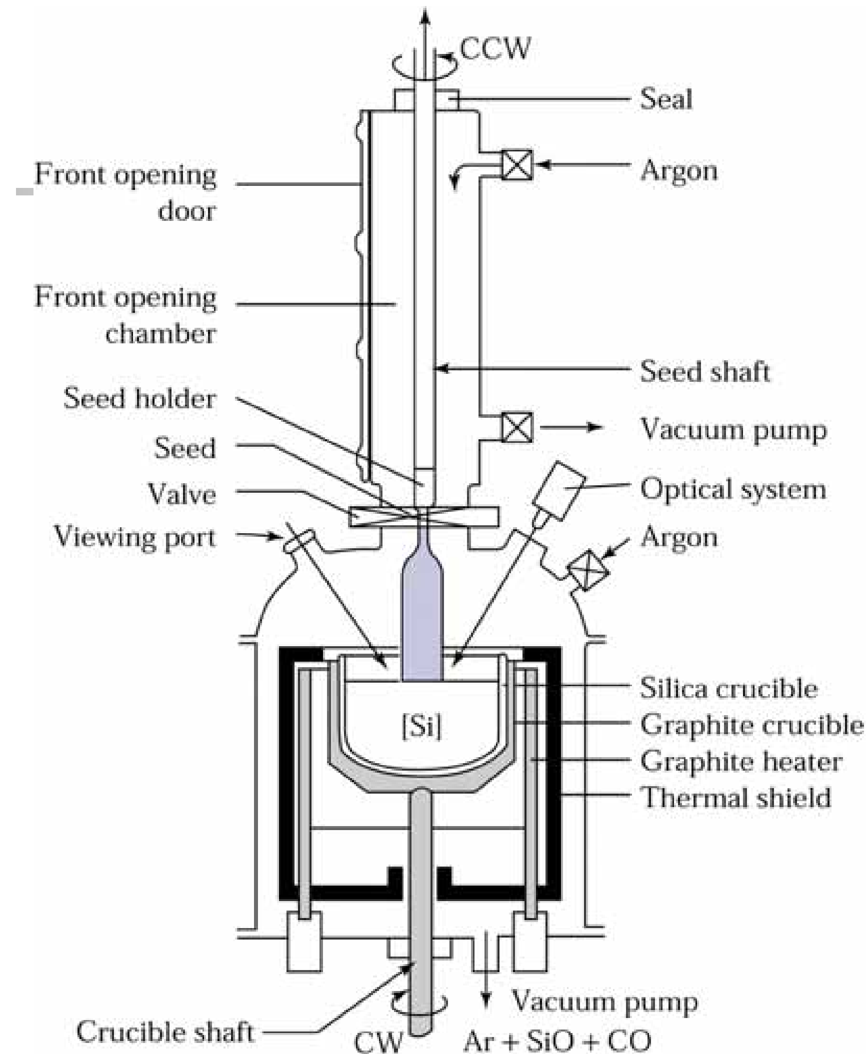
半導體材料成長

- 將純度不高之SiO_2在高溫下以碳還原成中純度之Si，然後利用HCl使其反應成SiHCl3的液體，再利用其沸點不同之特性加以蒸餾，最後形成高純度之Si塊
- 在融融狀態下以種晶在極慢的速度下拉晶
- 拉晶的方式區分為水平式（Bridgman)與垂直式 (Czochralski)

> 50% market for growing GaAs

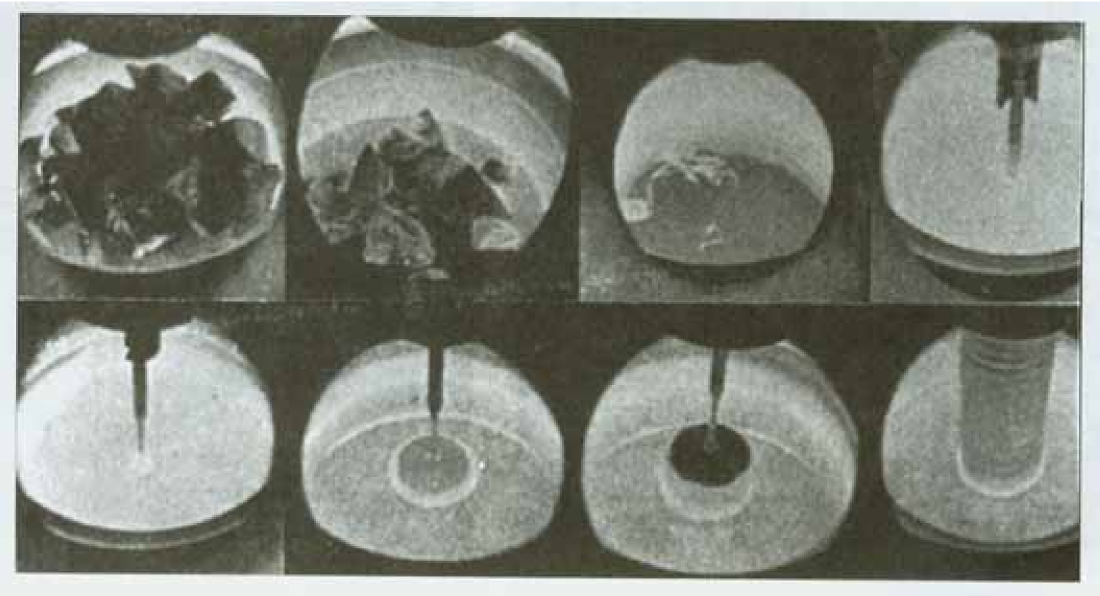


Schematic of a horizontal Bridgman growth system

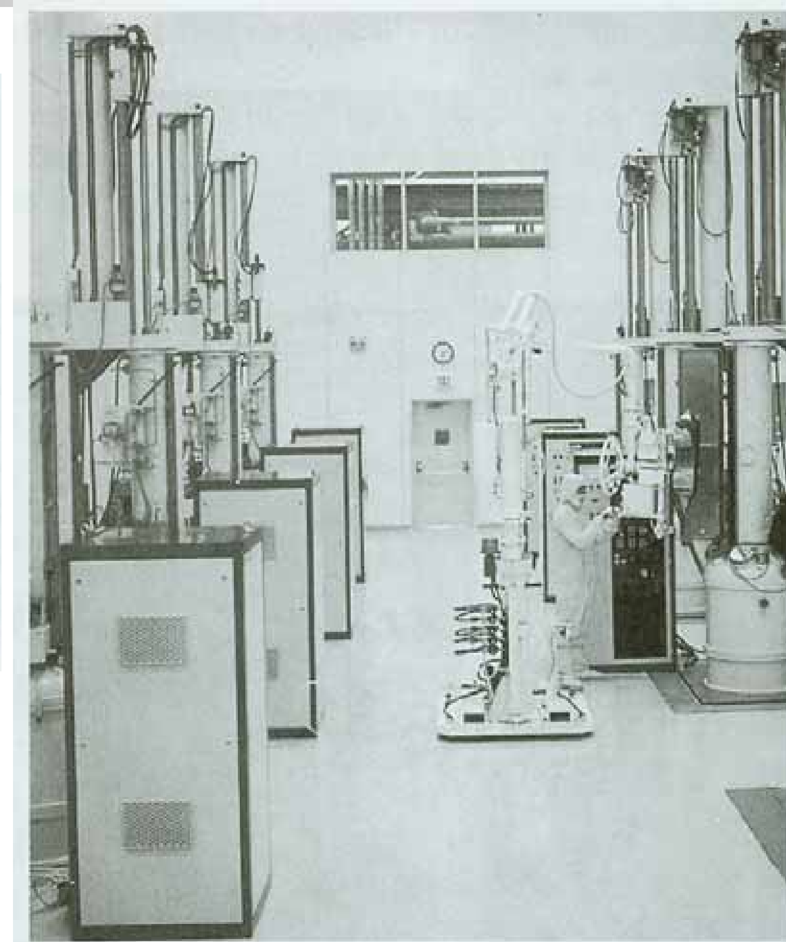


Simplified schematic drawing of the Czochralski puller. Clockwise (CW), counterclockwise (CCW).

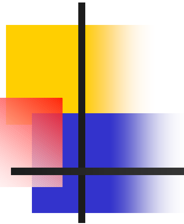
Czochralski Growth



Time lapse sequence of boule being pulled from the melt in a Czochralski growth

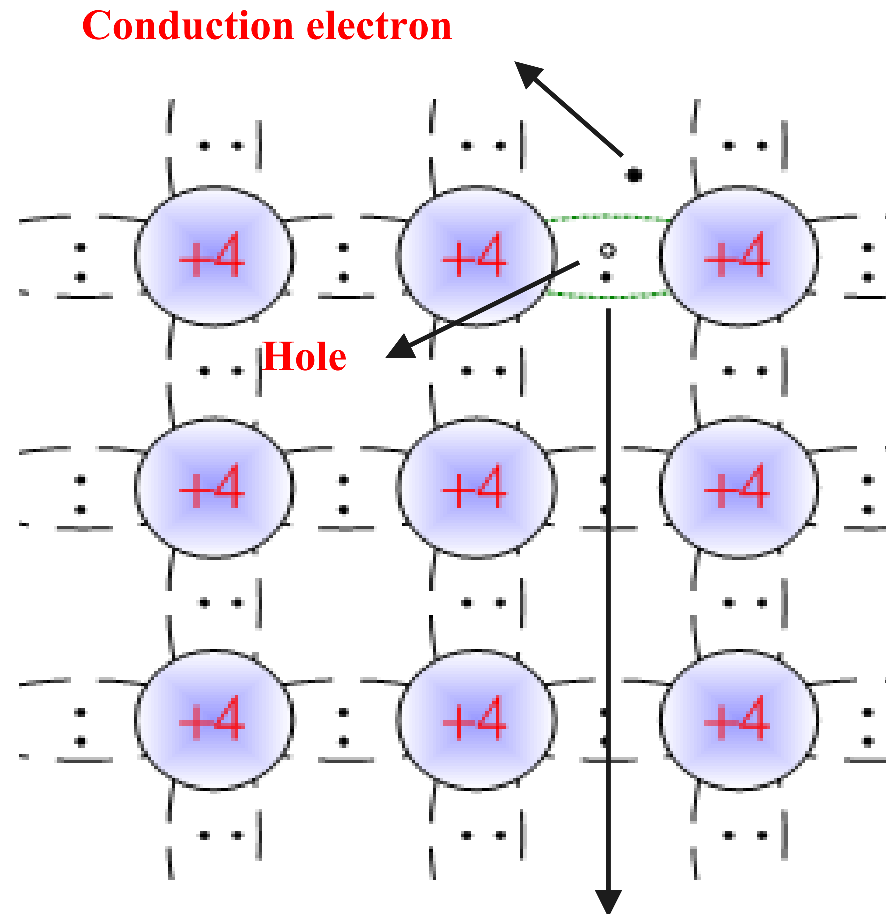


A 200-mm silicon growth facility



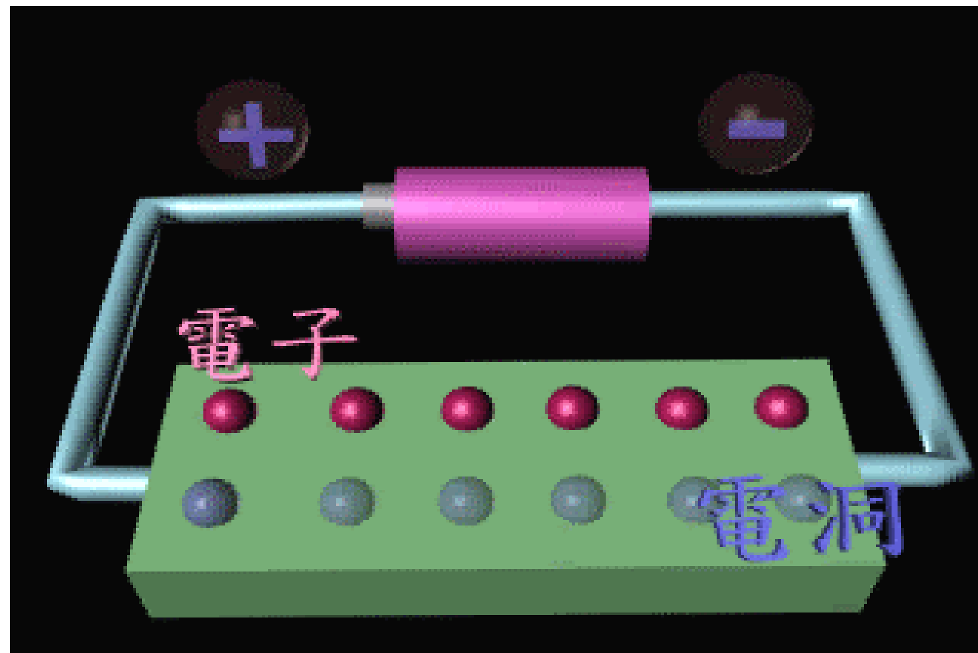
Carriers of Semiconductor

- **Electron and Hole**
  - Covalent band is broken at room temperature
    - Produce the free electron
    - Empty position – hole
  - Both electron and hole are called "carriers"



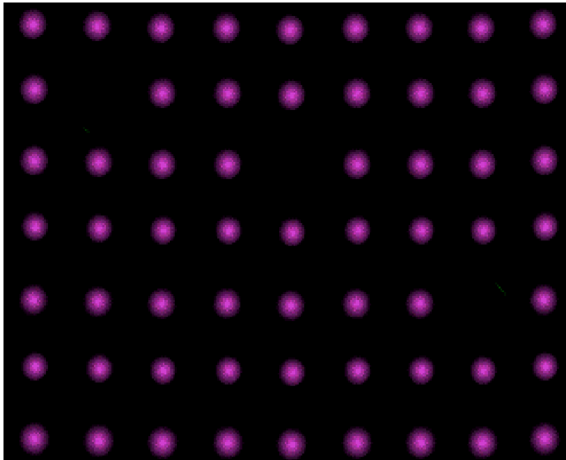
Carriers of Semiconductor

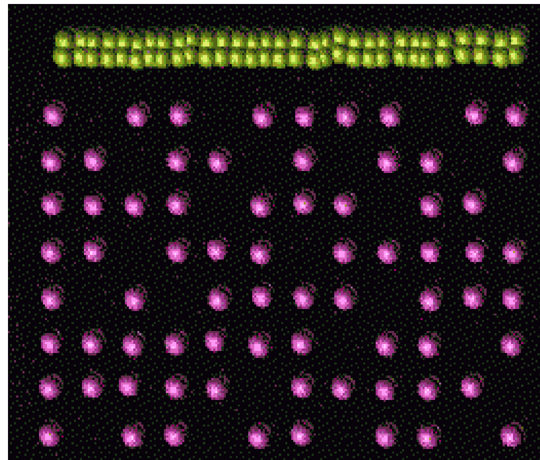
- **Electrons – negative charge**
- **Holes – positive charge**
  - The movement of carriers cause current in semiconductor

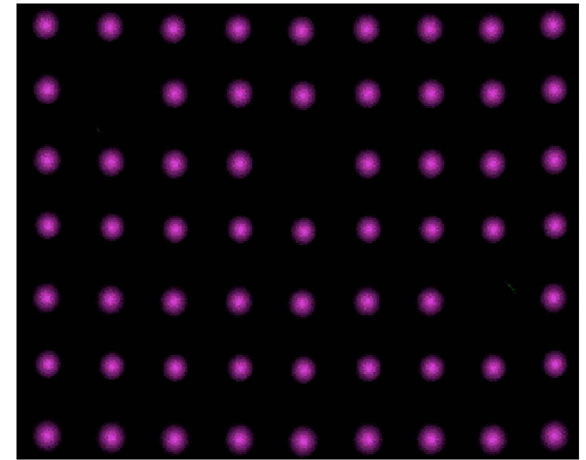


Ways of Doping

- **Intrinsic semiconductor**
  - Bad conductivity
- **Doping**
  - Substitutional impurity
  - Interstitial impurity
  - Interstitial-Substitutional impurity

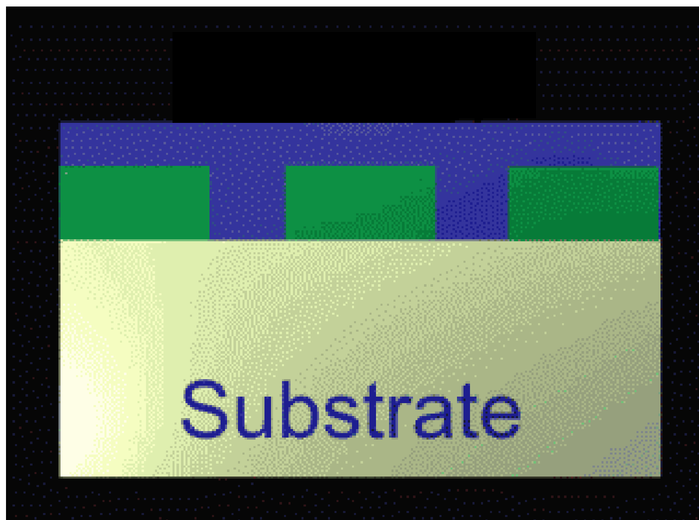


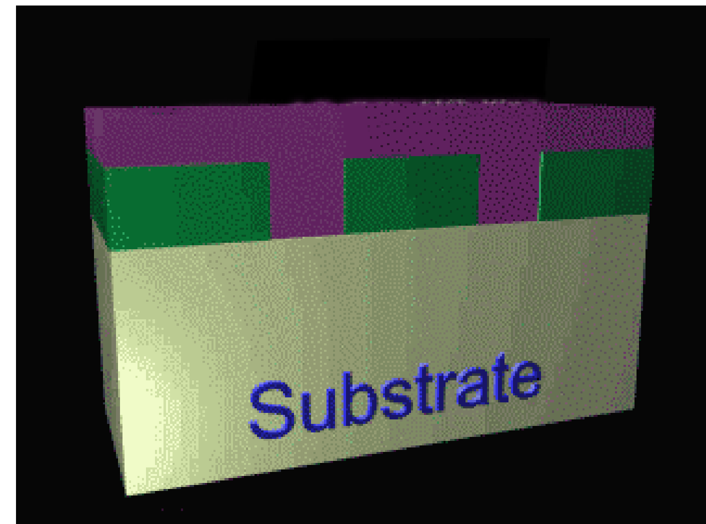




Doping Type

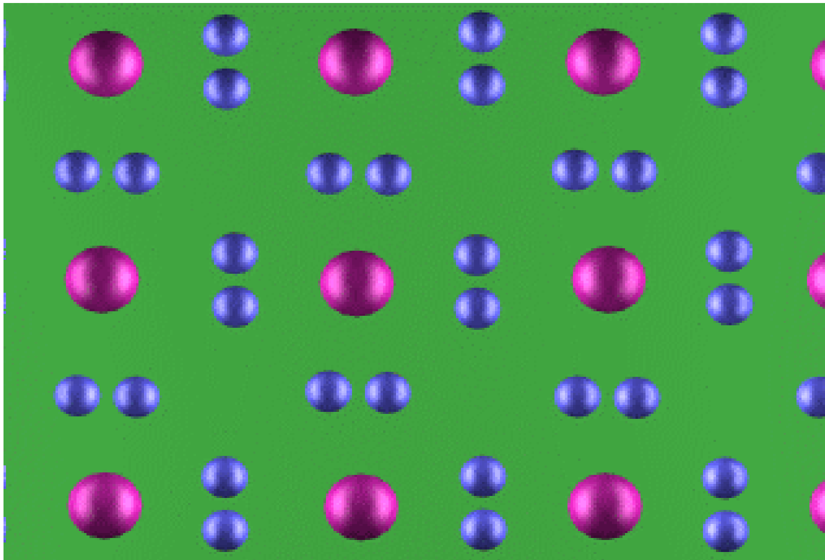
- **Extrinsic semiconductor**
  - Doped the impurities into intrinsic semiconductor
- **Acceptor**
  - p-type
- **Donor**
  - n-type

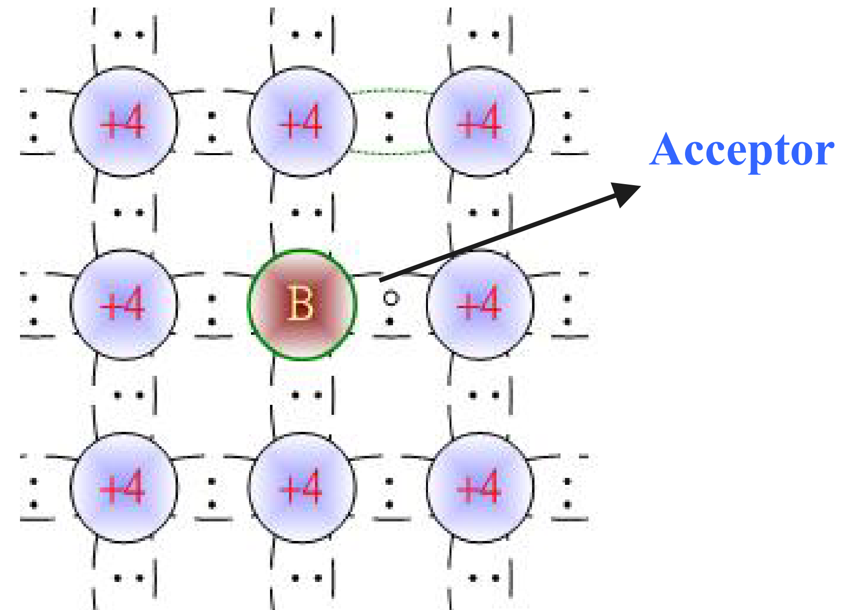




p-type Semiconductor

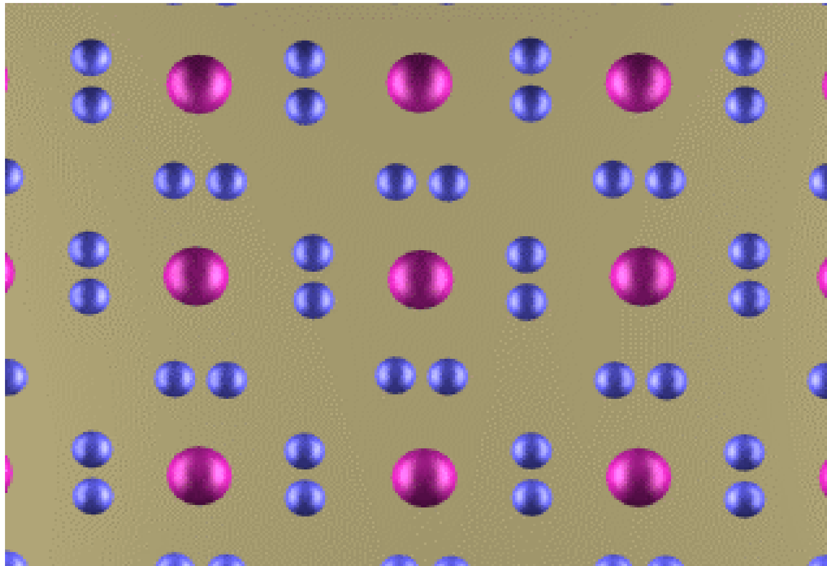
- **Acceptor**
  - Adding the element of Group III (B, Al)
    - Accept electron
  - Majority carrier – holes

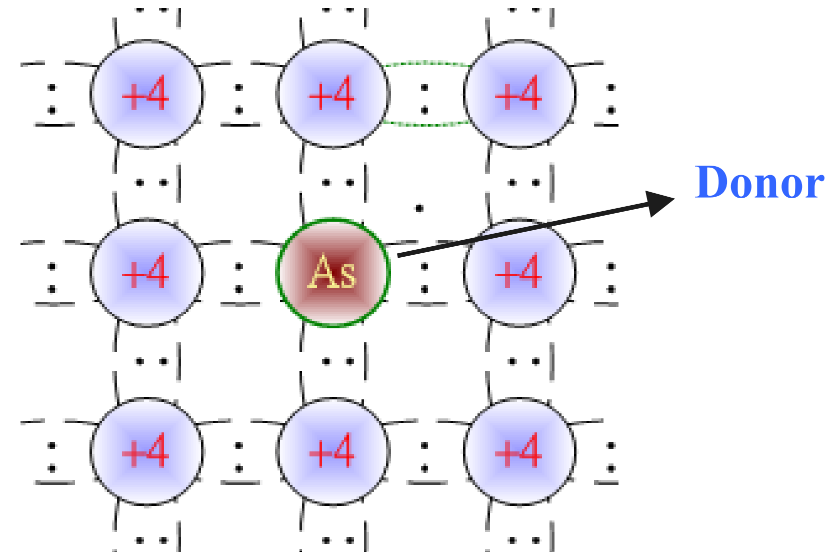




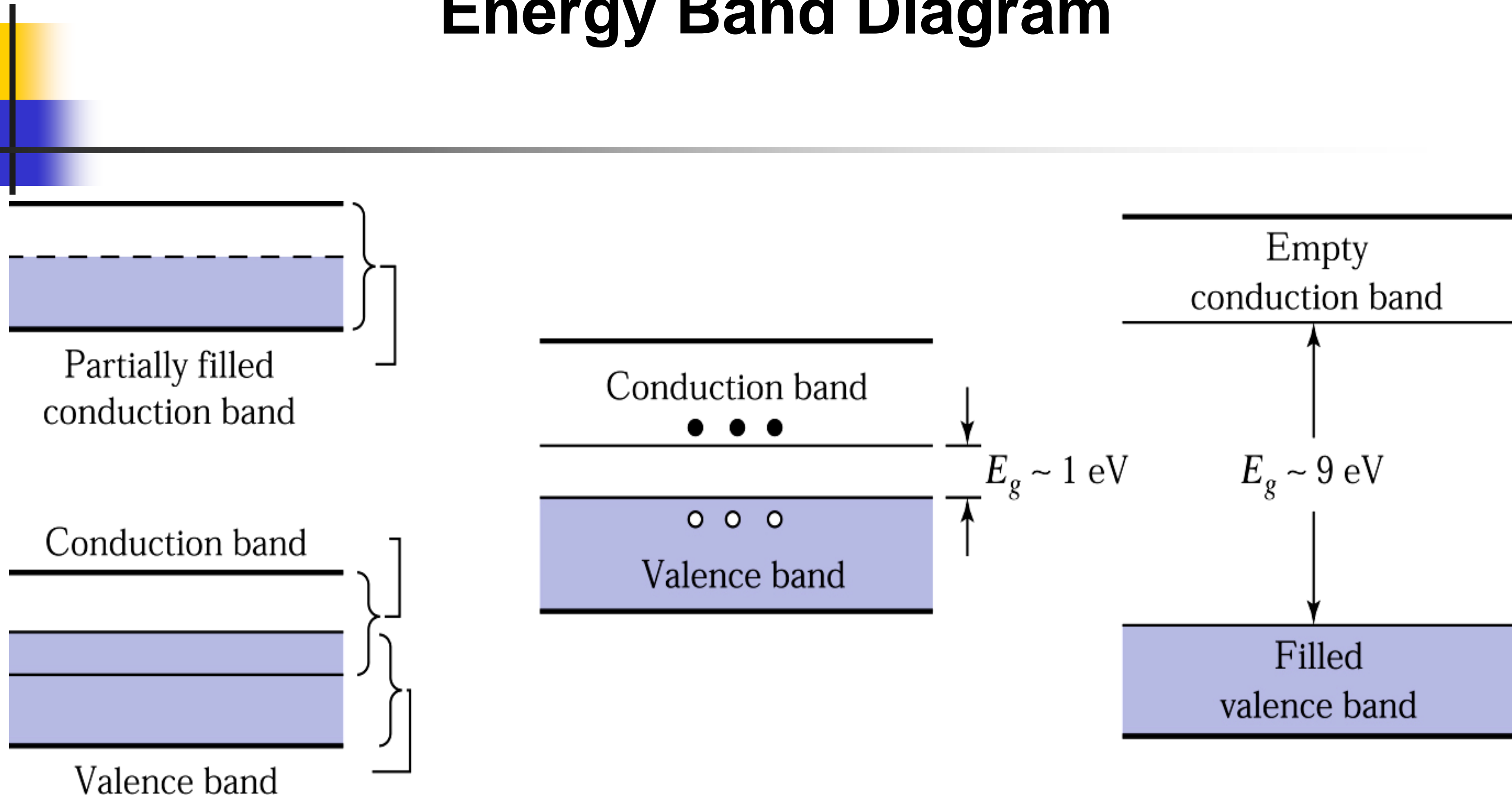
n-type Semiconductor

- **Donor**
  - Adding the element of Group V (P, As)
    - Supply electron
  - Majority carrier – electrons





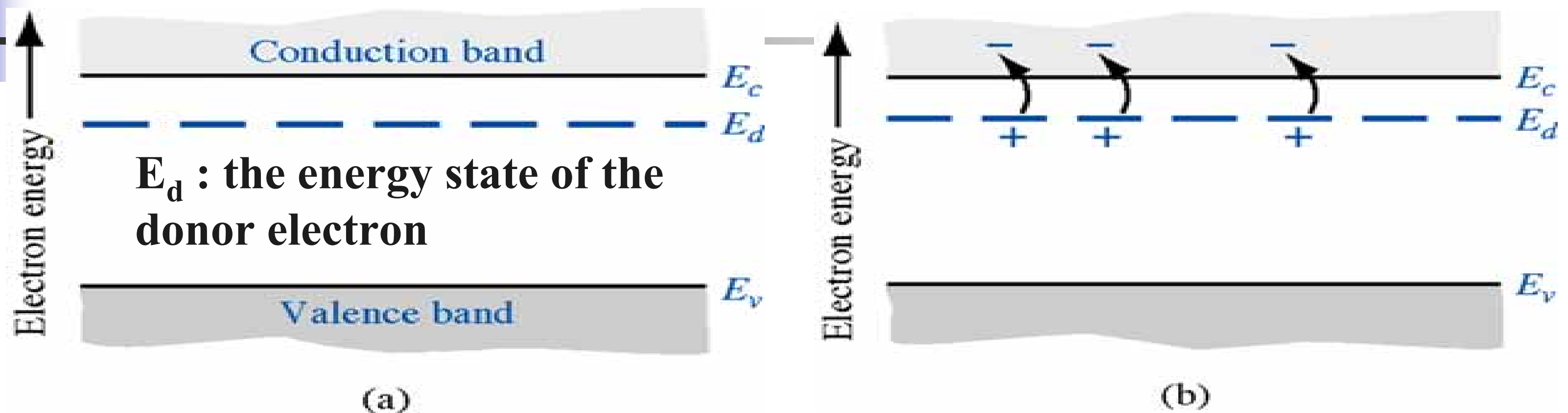
Energy Band Diagram



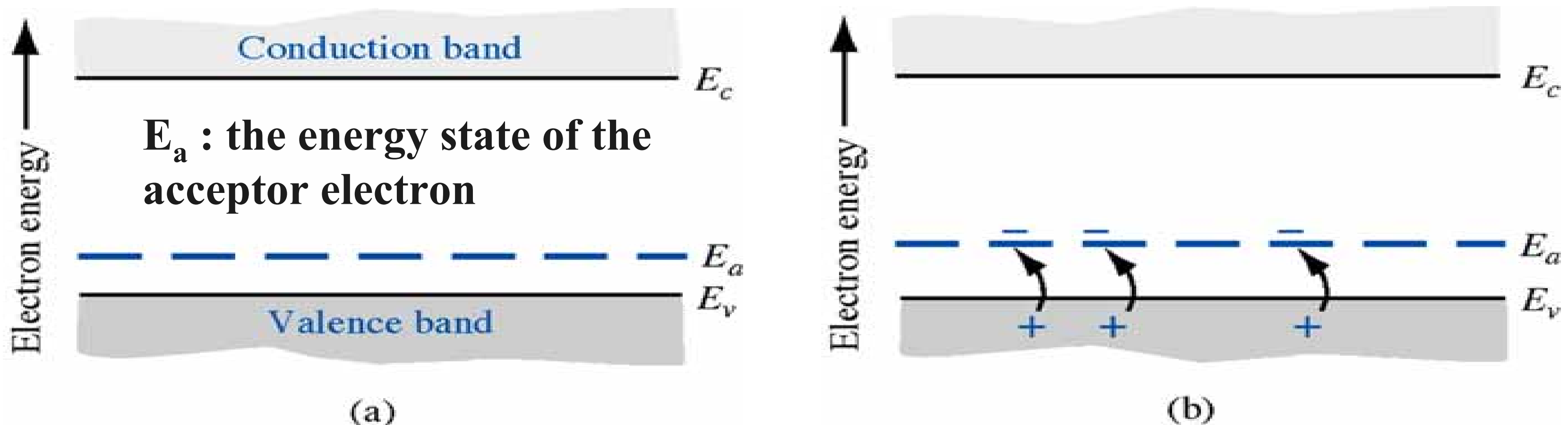
Schematic energy band representations of (*a*) a conductor with two possibilities (either the partially filled conduction band shown at the upper portion or the overlapping bands shown at the lower portion), (*b*) a semiconductor, and (*c*) an insulator.

Energy-Band Diagram

Donor & Acceptor Energy State



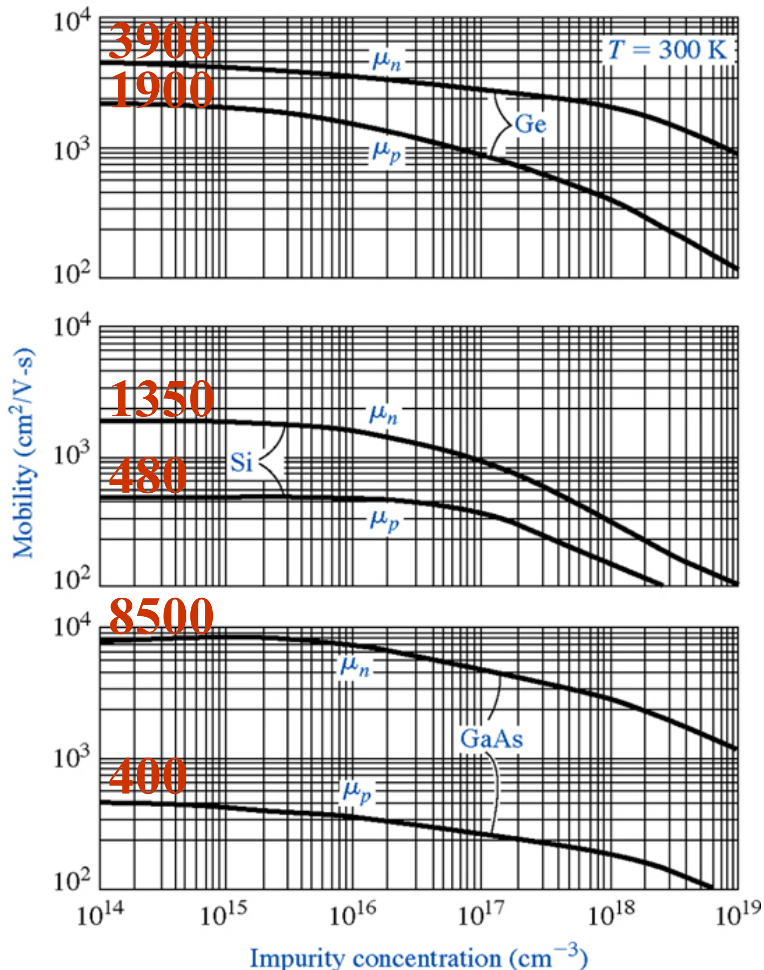
The energy-band diagram showing (a) the discrete donor energy state and (b) the effect of a donor state being ionized.



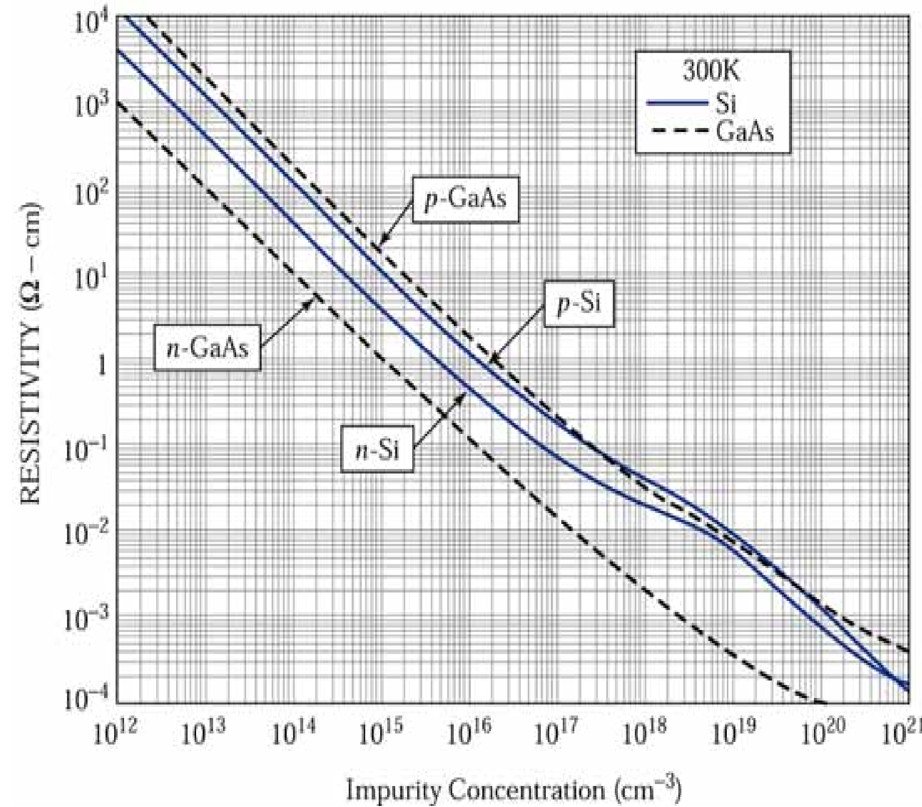
Energy-band diagram showing (a) the discrete acceptor energy state and (b) the effect of a acceptor state being

Mobility and Resistivity

Mobilities and diffusivities in Si and GaAs at 300 K as a function of impurity concentration.



Resistivity versus impurity concentration for Si and GaAs.



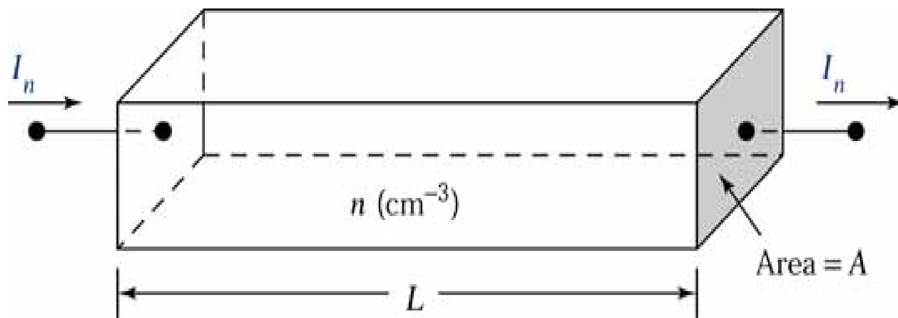
$$\rho \equiv \frac{1}{\sigma} = \frac{1}{q(n\mu_n + p\mu_p)}$$

Measurement of Resistivity

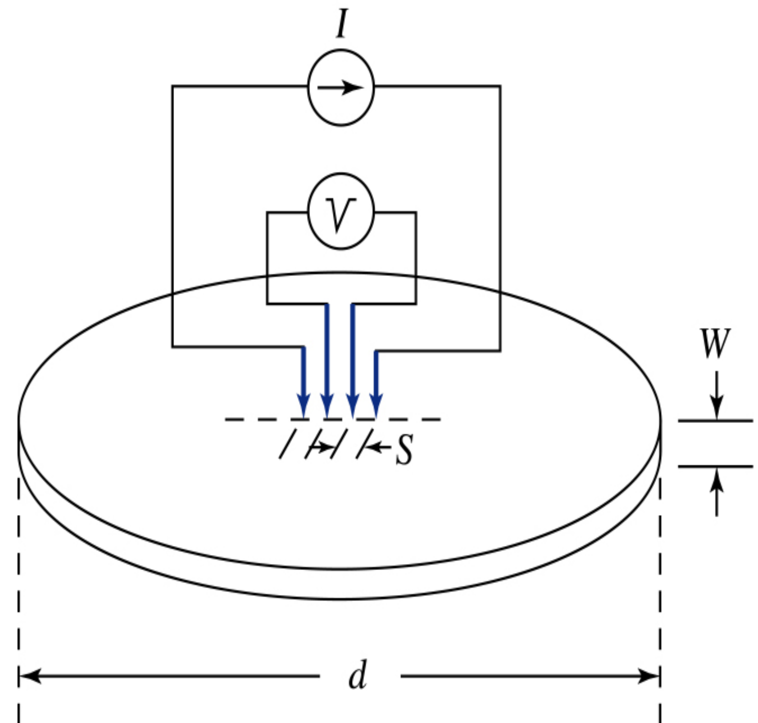
$$J_{drf} = q(\mu_n n + \mu_p p)E = \sigma E$$

$$\rho \equiv \frac{1}{\sigma} = \frac{1}{q(n\mu_n + p\mu_p)} \qquad (\Omega\text{-cm})$$

$$J = \frac{I}{A}\,;\, E = \frac{V}{L} \Rightarrow V = \left(\frac{L}{\sigma A}\right)I = IR$$

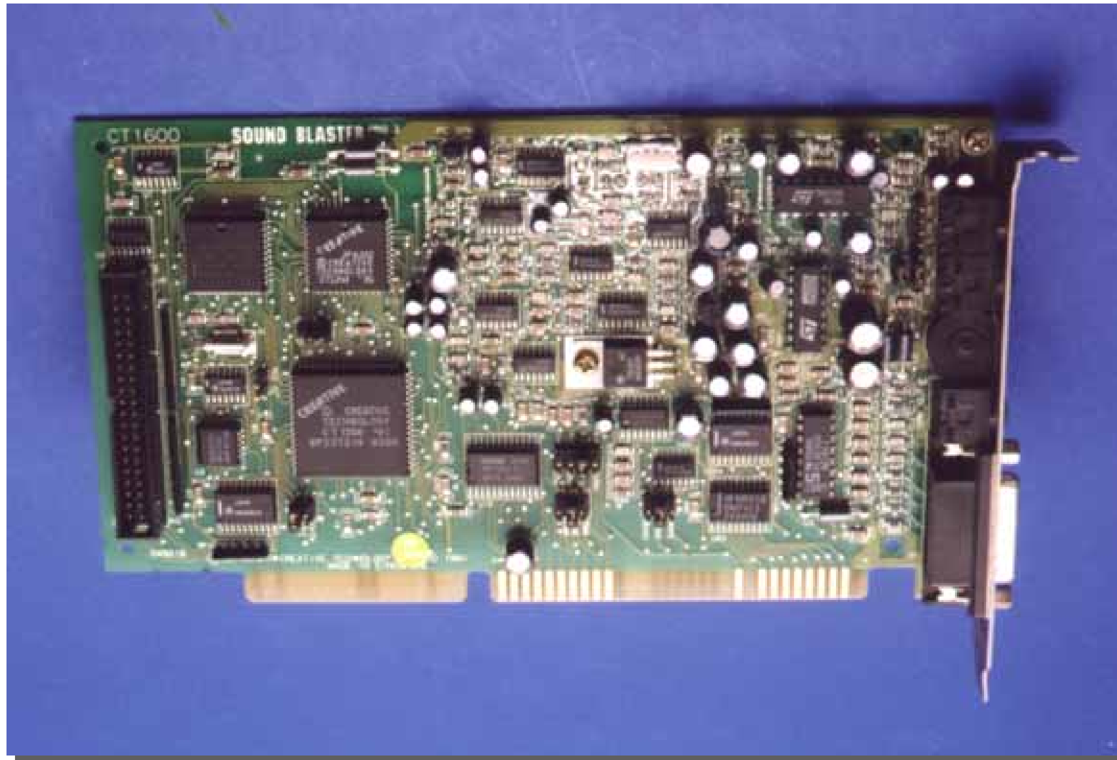


Current conduction in a uniformly doped semiconductor bar with length *L* and cross-sectional area *A*.



Measurement of resistivity using a four-point probe.

Semiconductor Devices
- Components on Printed Circuit Board



Circuit types: Analog & Digital Circuits
Component types: Passive & Active

Passive Component Structures
- IC Resistor Structures: Parasitic Resistor Structures

Integrated circuit resistors. All narrow lines in the large square area have the same width W, and all contacts are the same size.

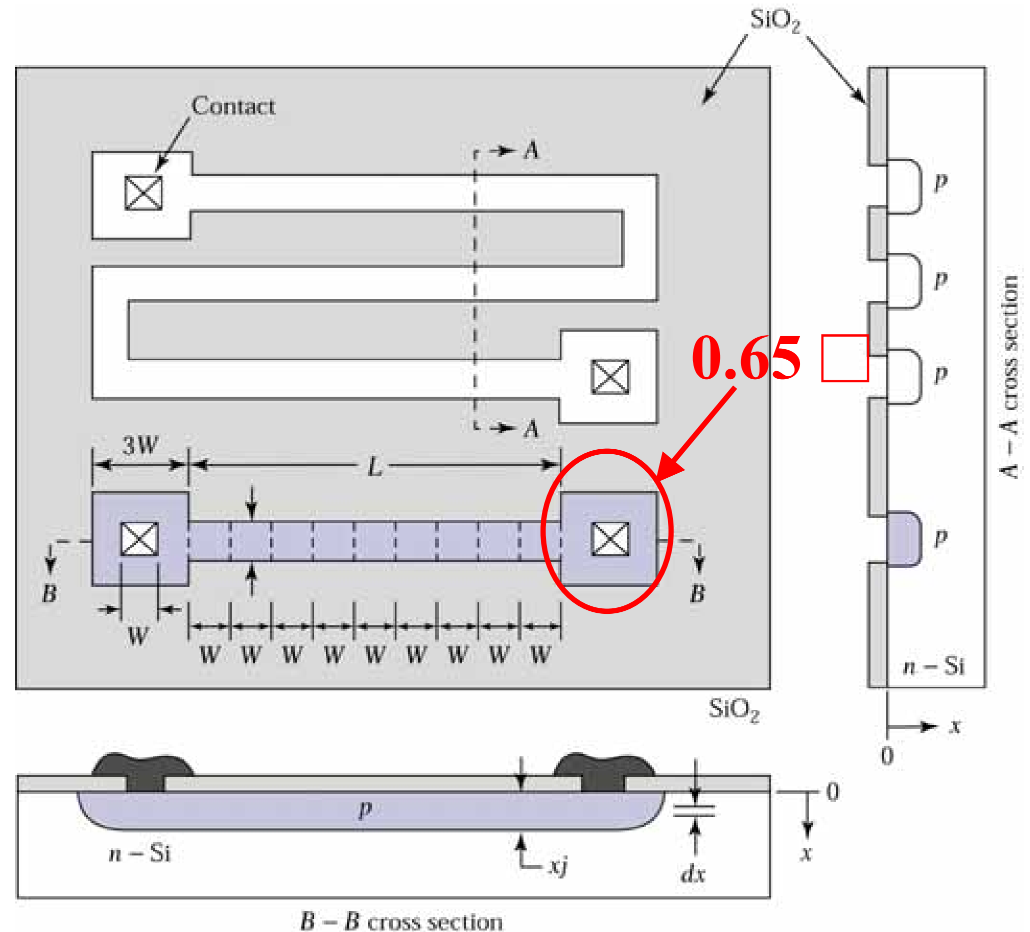
$$R \equiv \frac{1}{G} = \frac{L}{W}\left(\frac{1}{g}\right)$$

where 1/g : sheet resistance (Ω/□)

Example: L=90 μm; W=10 μm;

1/g=1 kΩ/□

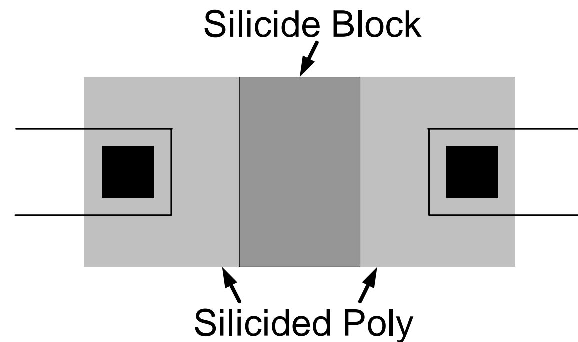
R=(9+0.65*2)* 1 kΩ/□=10.3 kΩ

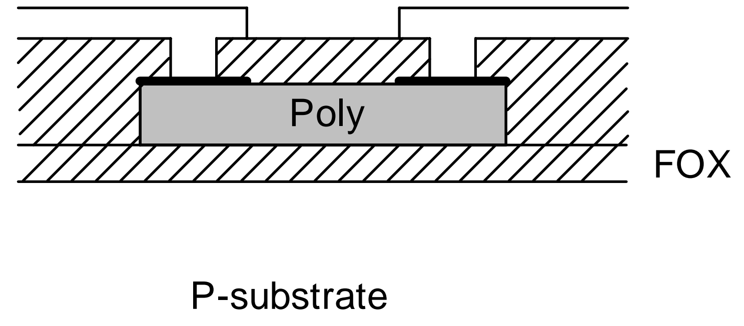


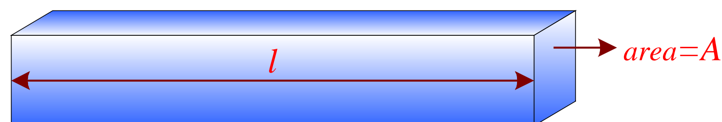
Examples of Resistor Structures in ICs

Resistor

- Polysilicon resistor
  - is doped on an IC chip
  - Linear
    - Resistance is determined by length, area, and the resistivity of the material type







symbol

Resistor

- **Interconnect Resistance**

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Passive Component Structures

Examples of Capacitors Structures in ICs

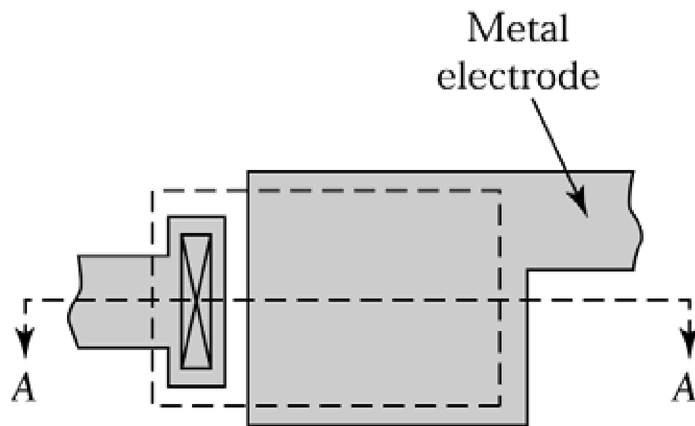
(*a*) Integrated MOS capacitor. (*b*) Integrated *p-n* junction capacitor.

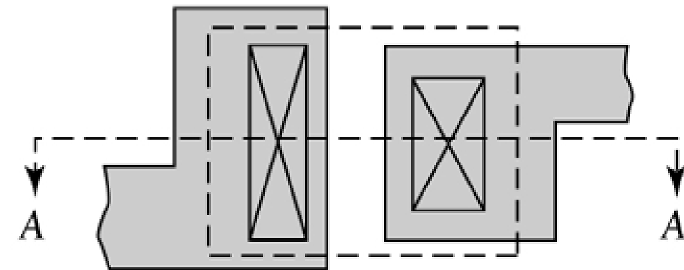
$$C = \frac{\epsilon_{ox}}{d} \quad (F/cm^2) \quad ; \quad \epsilon_{ox} = \epsilon_r \epsilon_0 = 3.9 \epsilon_0$$

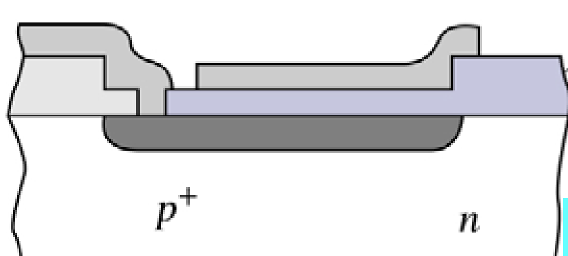
where ϵ_{ox}: dielectric permittivity of SiO_2

ϵ_r: dielectric constant of $SiO_2 = 3.9$

ϵ_0: permittivity of free space (8.85×10^{-14} F/cm)



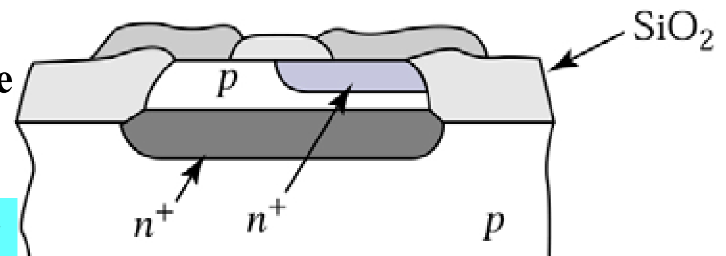




(a)

Increase the dielectric constant

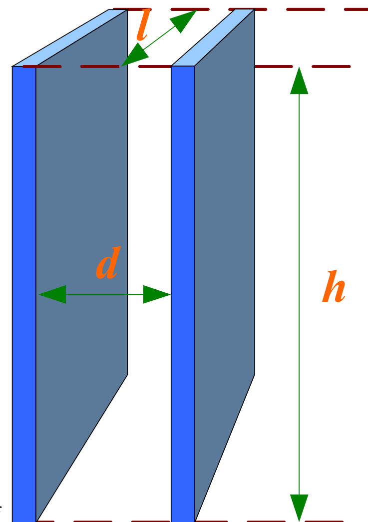
Si_3N_4 ($\epsilon_r = 7$) or Ta_2O_5 ($\epsilon_r = 25$)

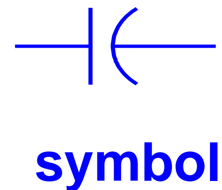


(b)

Capacitor

- Charge storage device
  - Memory Devices, esp. DRAM
  - Two boards of semiconductor material as a capacitor
- Capacitances
  - are proportional to the area (A=h*l)
  - are inverse proportional to the distance



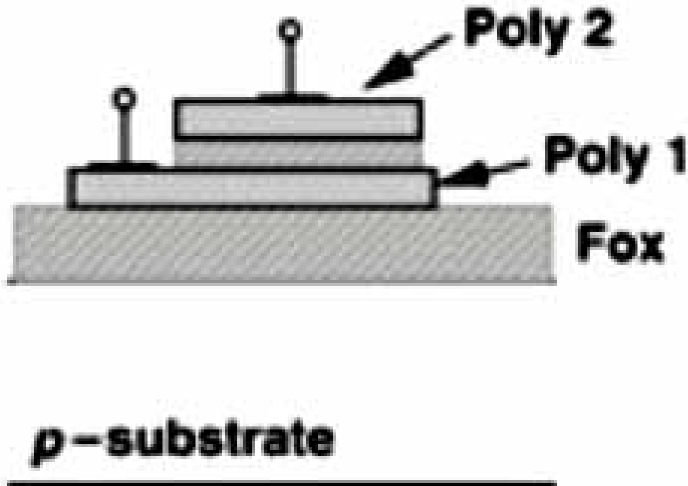


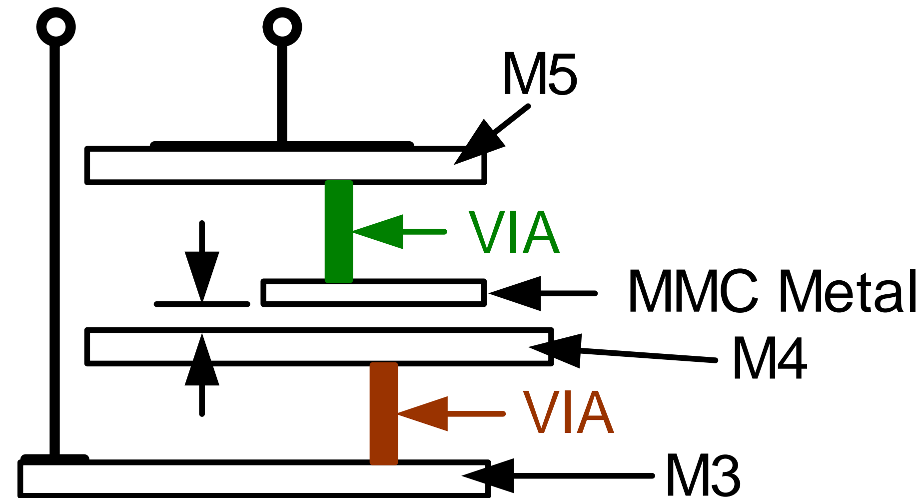
symbol

$$C = \in_r \in_0 \frac{hl}{d} \quad (F)$$

Capacitor

- Poly–poly (double poly process)
  - Middle value
  - Better noise immunity
- MMC (metal/metal capacitor)





Passive Component Structures

Examples of Inductors Structures in ICs

Quality factor: Q = Lω/R

The higher the Q values; the lower the loss from resistance, hence the better the performance of the circuits.

There are some approaches to improve the Q values:

(1) Reduce C_p : use low ϵ_{ox} material

(2) Reduce R_1 : use thick film metal (e.g. Cu, Au)

(3) Reduce $R_{sub\ loss}$: use insulating substrate (SOI, quartz)

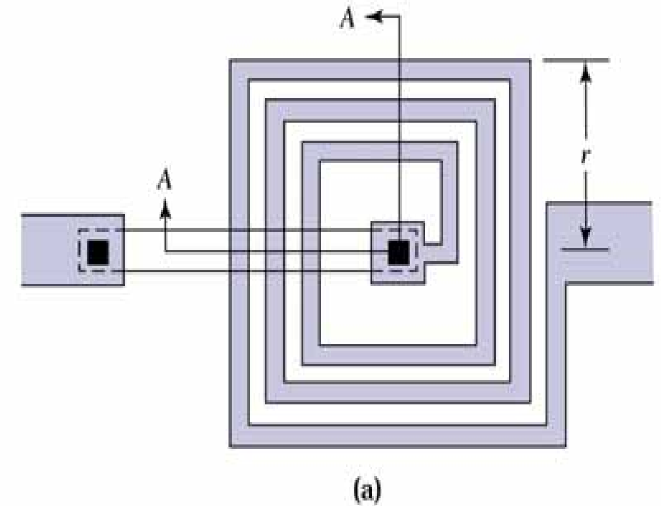
An estimated inductance of the square planar spiral inductor :

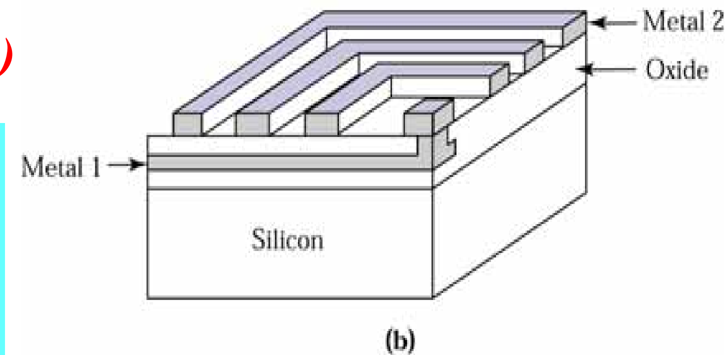
$$L \approx \mu_0 n^2 r \approx 1.2\times10^{-6} n^2 r$$

where μ_0 : permeability in vacuum

$$= (4\pi\times10^{-7} H/m)$$

n : the number of turns



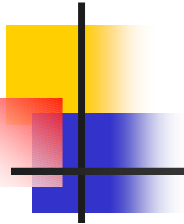


(*a*) Schematic view of a spiral inductor on a silicon substrate. (*b*) Perspective view along *A-A*'

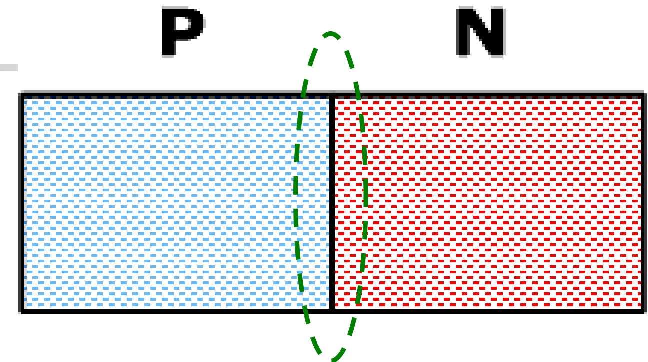
Active Component Structures

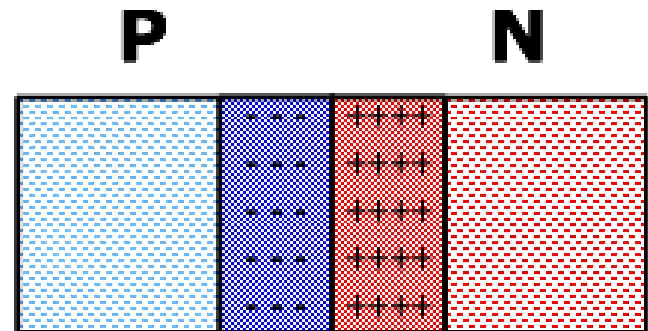
- The pn Junction Diode
- The Bipolar Junction Transistor (BJT)
- The Metal-Oxide-Semiconductor FET (MOSFETs)
- Complementary MOSFET (CMOS)

PN Junction

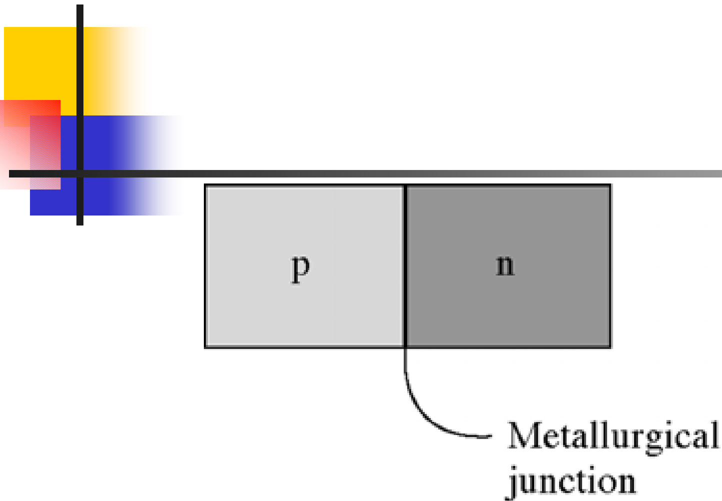


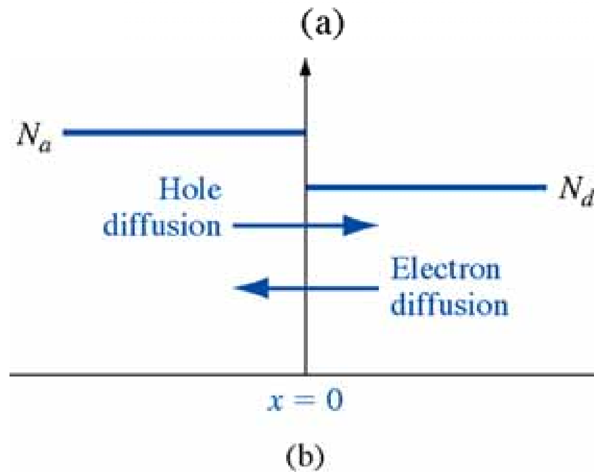
- **Diode**
  - **p region**
    - Doped with acceptor impurities
    - The positive charges atoms left
  - **n region**
    - Doped with donor impurities
    - The negative charges atoms left
  - **Space charge region in thermal equilibrium**
    - Also called depletion region
    - No mobile carrier exists
    - Two forces exactly balance each other
      - No current

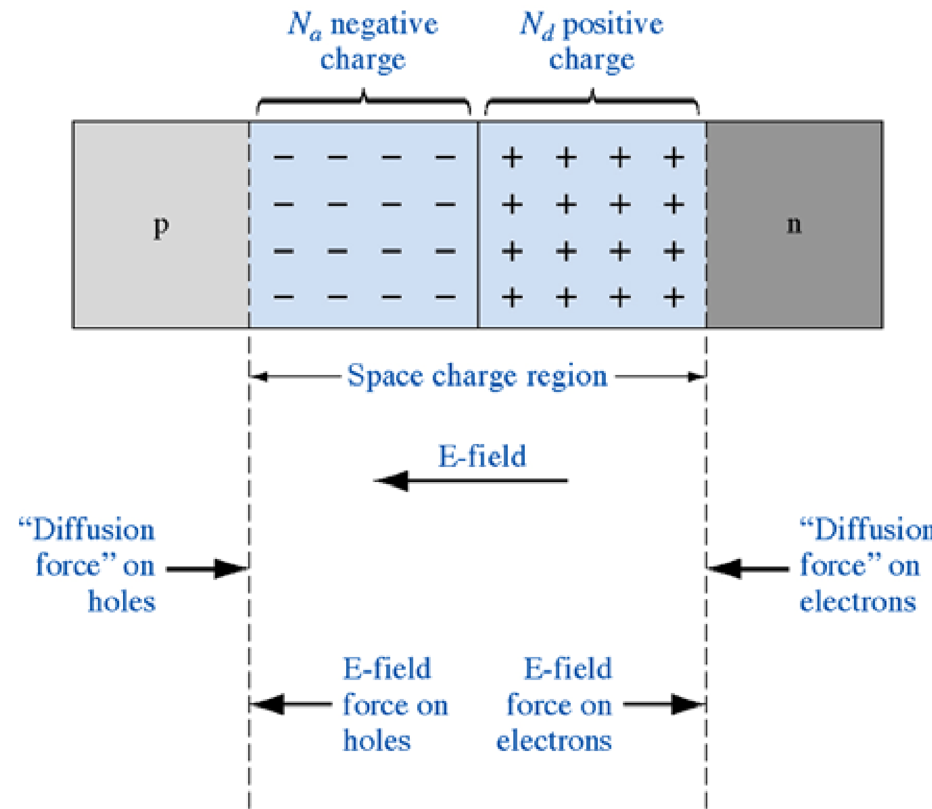




PN Junction





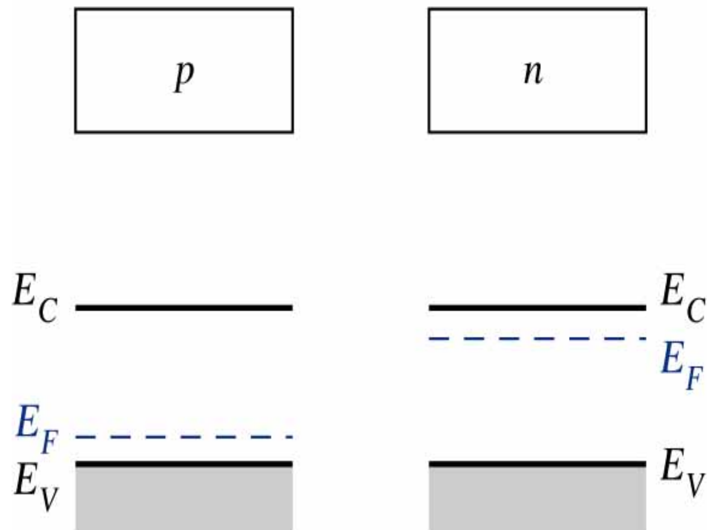


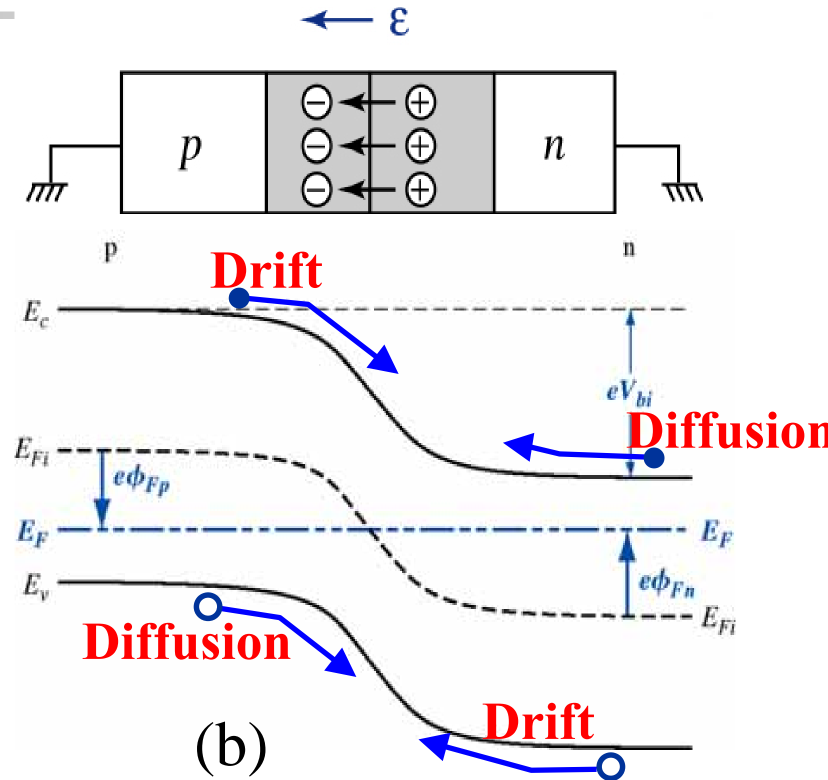
(a) **Simplified geometry of a pn junction;**

(b) **Doping profile of an ideal uniformly doped pn junction**

The space charge region, the electric field, and the forces acting on the charged carriers.

Energy Band Diagram of the PN Junction



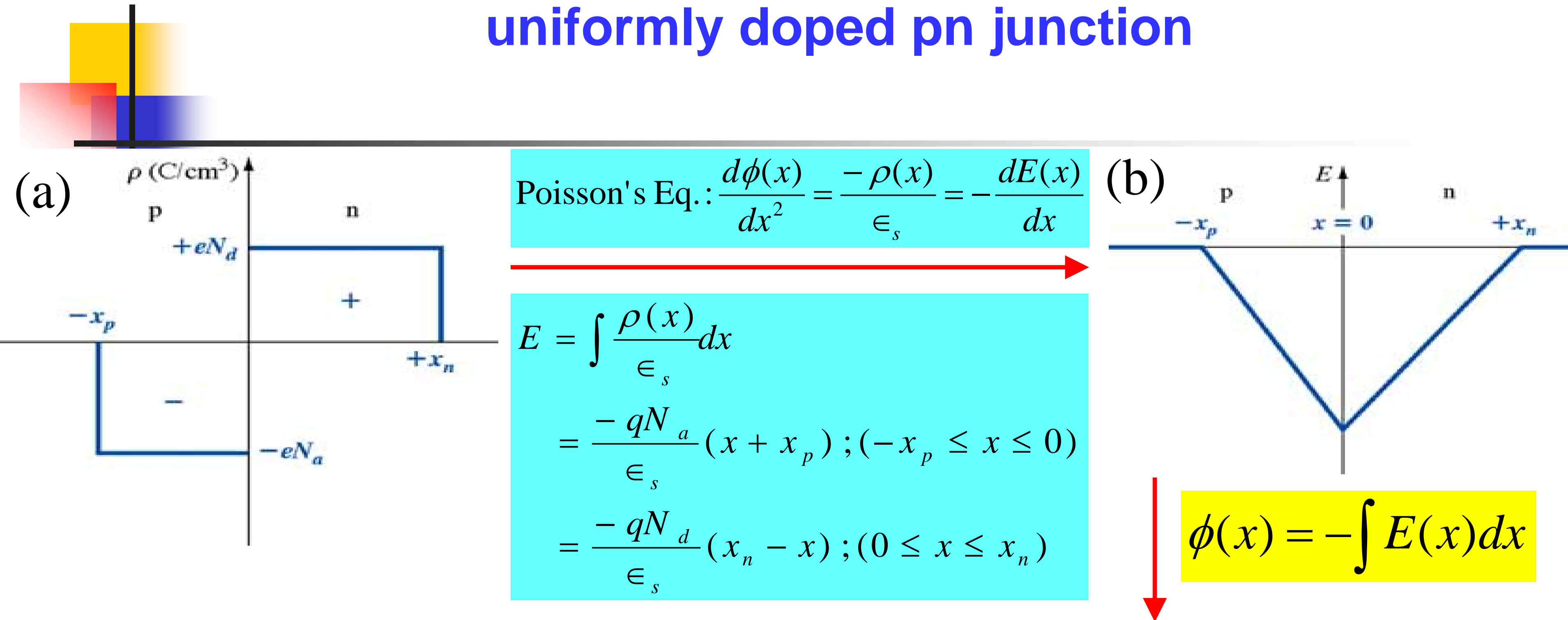


(*a*) Uniformly doped *p*-type and *n*-type semiconductors before the junction is formed. (*b*) The energy band diagram of a *p*-*n* junction in thermal equilibrium.

Build-in voltage : $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) = V_t \ln\left(\frac{N_a N_d}{n_i^2}\right)$

Space Charge Density & Electric Field/Potential

uniformly doped pn junction



$$\phi(x) = -\int E(x)dx$$

(c)

p

n

ϕ

V_{bi}

$-x_p$ $x = 0$ $+x_n$

(a) The space charge density in a uniformly doped pn junction assuming the abrupt junction approximation

(b) Electric field in the space charge region in a uniformly doped pn junction

(c) Electric potential through the space charge region in a uniformly doped pn junction

Space Charge Density & Electric Field/Potential

One-sided abrupt junction

(a) One-sided abrupt junction (with $N_A >> N_D$) in thermal equilibrium.

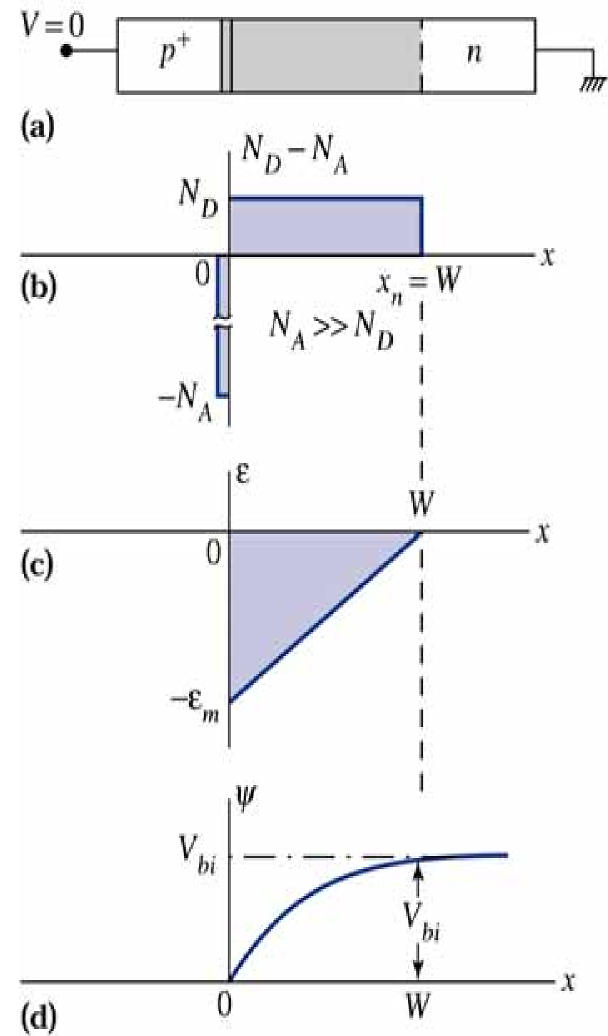
(b) Space charge distribution.

(c) Electric-field distribution.

(d) Potential distribution with distance, where V_{bi} is the built-in potential.

$$W = \left\{ \frac{2\in_s V_{bi}}{q} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2}$$

$$\cong x_n = \sqrt{\frac{2\in_s V_{bi}}{qN_d}}$$

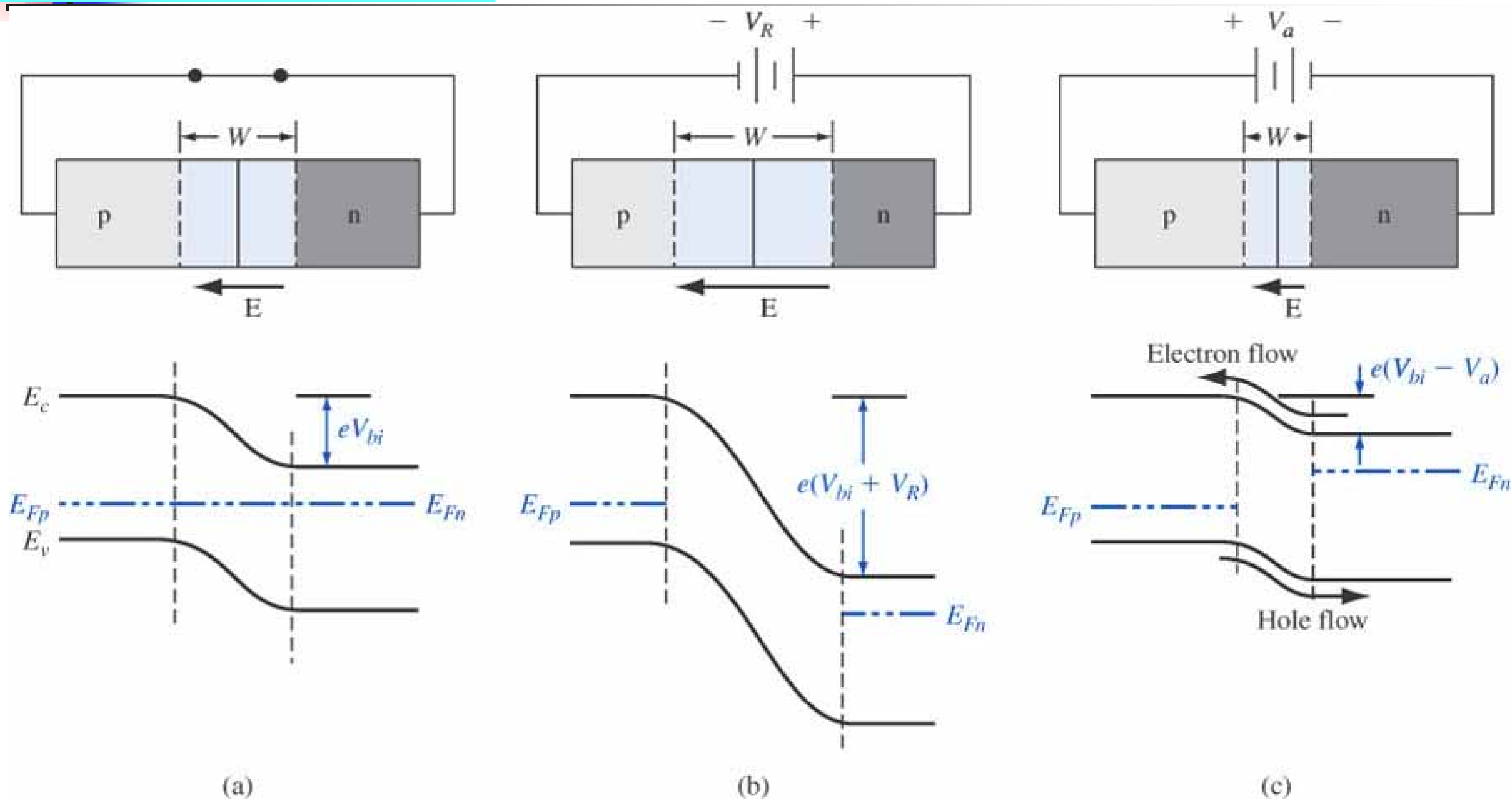


The Uniformly Doped pn Junction Diode

$$W = \left\{ \frac{2 \in_s V_{bi}}{q} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2}$$

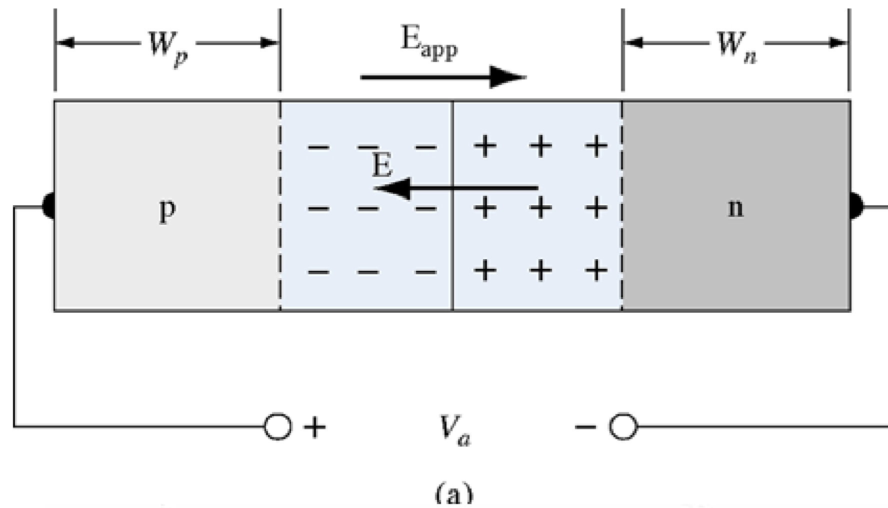
$$W = \left\{ \frac{2 \in_s (V_{bi} + V_R)}{q} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2}$$

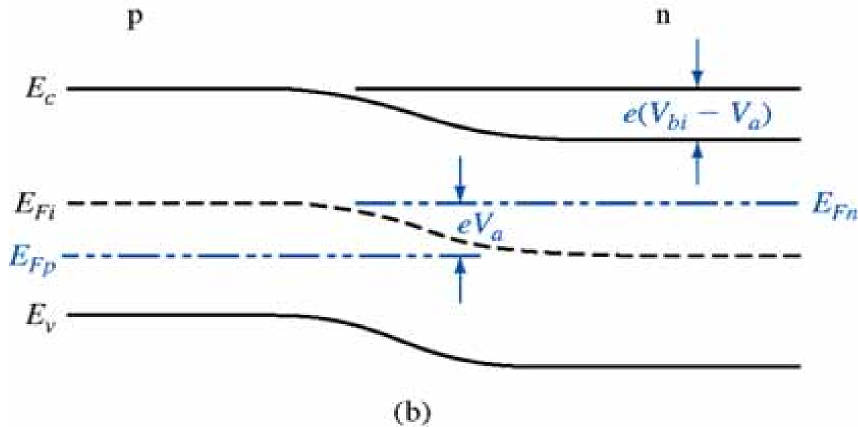
$$W = \left\{ \frac{2 \in_s (V_{bi} - V_a)}{q} \left[\frac{N_a + N_d}{N_a N_d} \right] \right\}^{1/2}$$

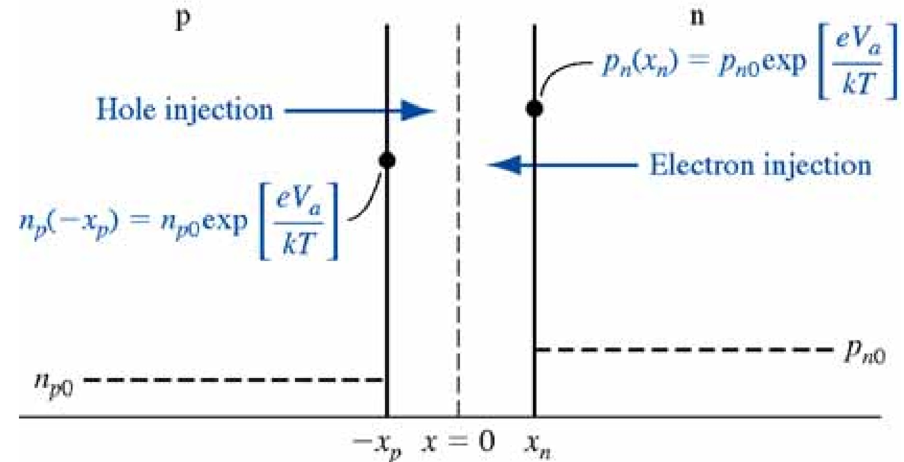


Schematic representation of depletion layer width and energy band diagrams of a *p-n* junction under various biasing conditions. (*a*) Thermal-equilbrium condition. (*b*) Reverse-bias condition. (*c*) Forward-bias condition.

Ideal Current-Voltage Relationship of Diode





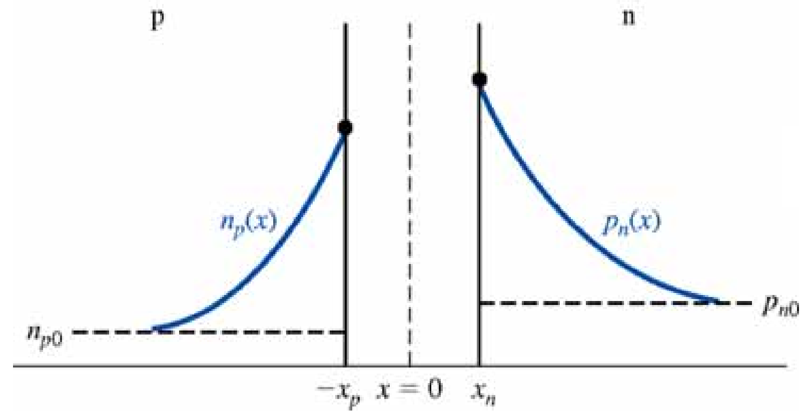


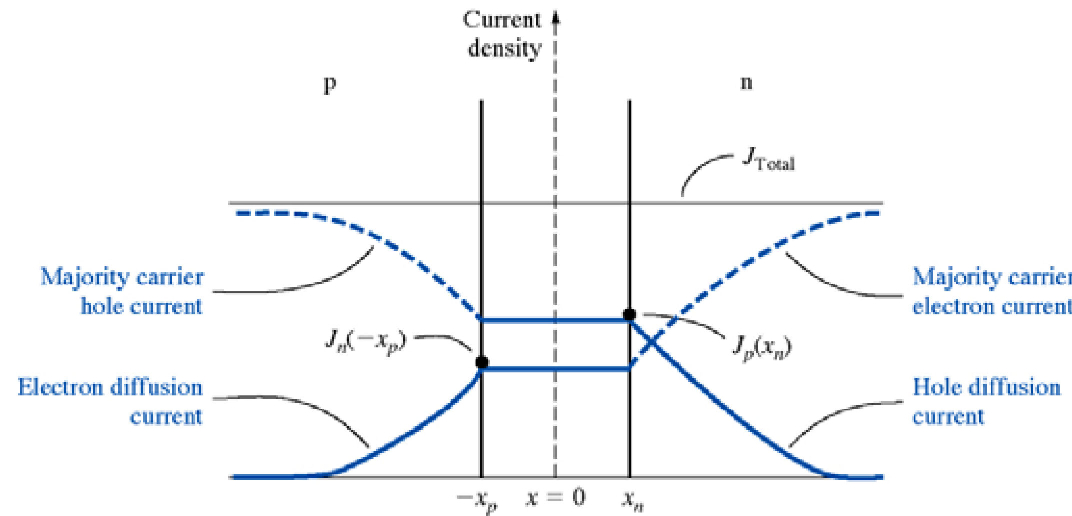
(a) A pn junction with an applied forward-bias voltage showing the directions of the electric field induced by V_a and the space charge electric field.

(b) Energy-band diagram of the forward-biased pn junction

Excess minority carrier concentrations at the space charge edges generated by the forward-bias voltage

Ideal PN Junction Current





Steady-state minority carrier concentrations in a pn junction under forward bias

Ideal electron and hole current components through a pn junction under forward bias.

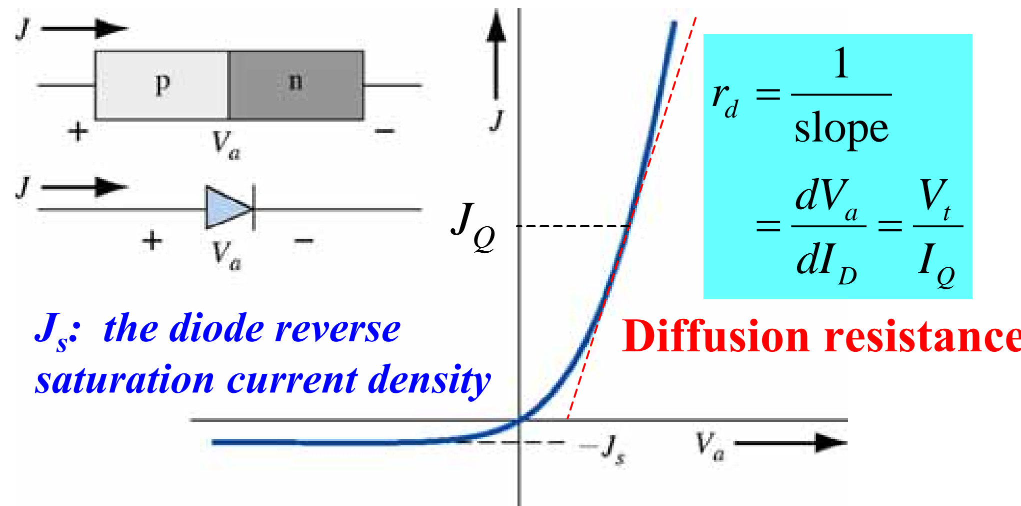
$$J_p(x_n) = \frac{qD_p p_{n0}}{L_p}[\exp(\frac{qV_a}{kT}) - 1]$$

$$J_n(-x_p) = \frac{qD_n n_{p0}}{L_n}[\exp(\frac{qV_a}{kT}) - 1]$$

$$J_D = J_p(x_n) + J_n(-x_p)$$

$$= [\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}][\exp(\frac{qV_a}{kT}) - 1]$$

$$= J_s[\exp(\frac{qV_a}{kT}) - 1] \approx J_s \exp(\frac{qV_a}{kT})$$



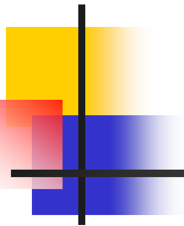
$$r_d = \frac{1}{\text{slope}} = \frac{dV_a}{dI_D} = \frac{V_t}{I_Q}$$

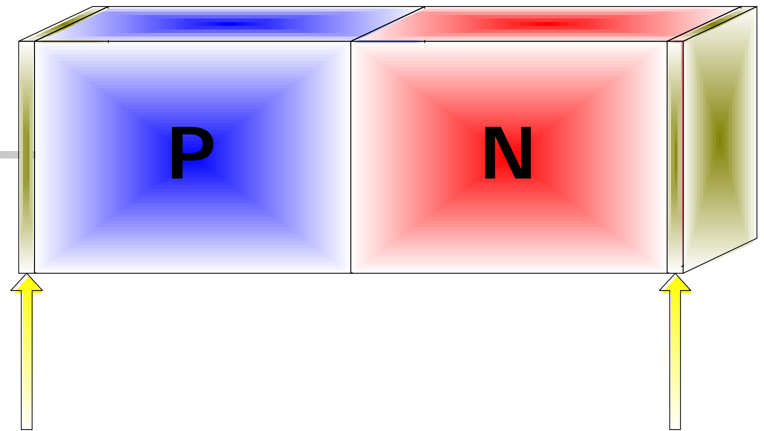
Diffusion resistance

J_s: the diode reverse saturation current density

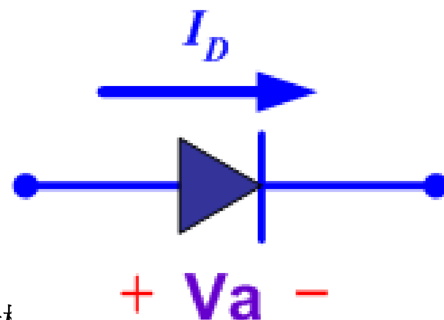
Ideal I-V characteristic of a pn junction diode

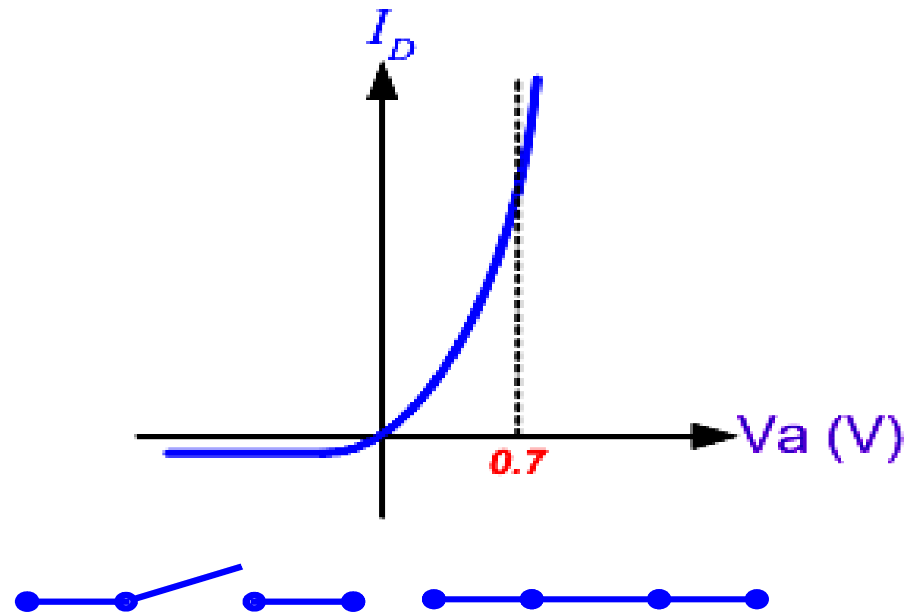
PN Junction Diode





- **Switch**
  - Forward biased (Va > 0)
    - Short
      - Current
  - Reverse biased (Va < 0)
    - Open
      - No current





Fabrication Processes of PN Junction Diode

(a) The wafer after the development.

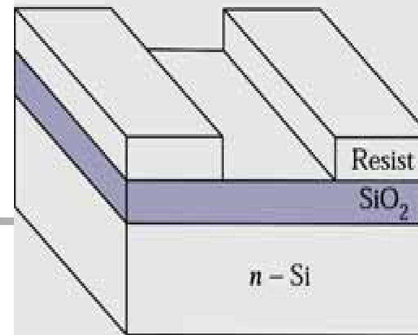
(b) The wafer after SiO_2 removal.

(c) The final result after a complete lithography process.

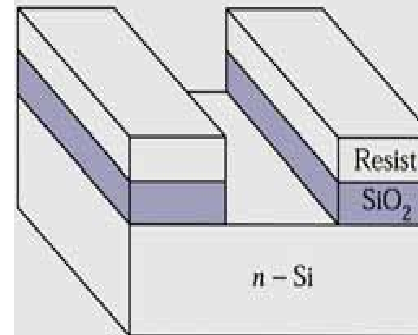
(d) A *p-n* junction is formed in the diffusion or implantation process.

(e) The wafer after metallization.

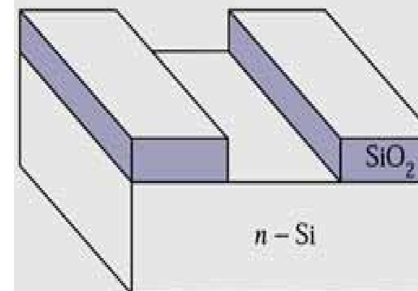
(f) A *p-n* junction after the compete process.



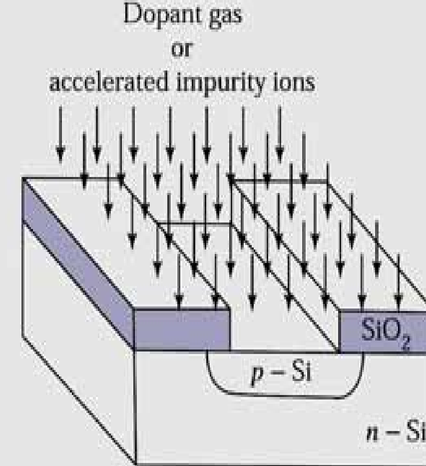
(a)



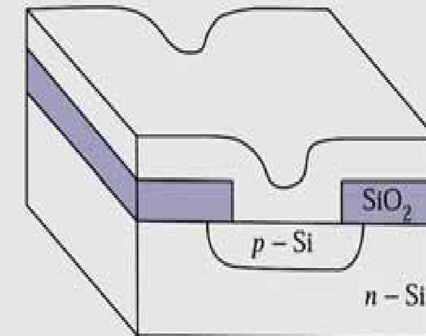
(b)



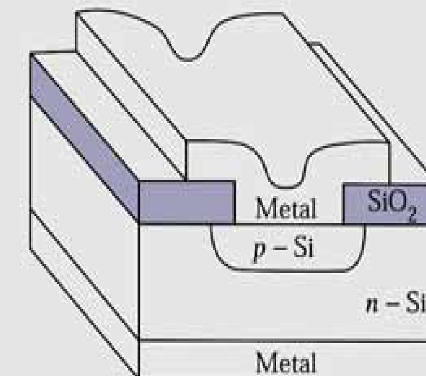
(c)



(d)



(e)



(f)

Application of Diode

- **Diode**
  - **Used for protection circuit**
    - In substrate
      - Remain reverse biased
    - In n-well
      - Prevent forward pn junction
        - Substantial current flow