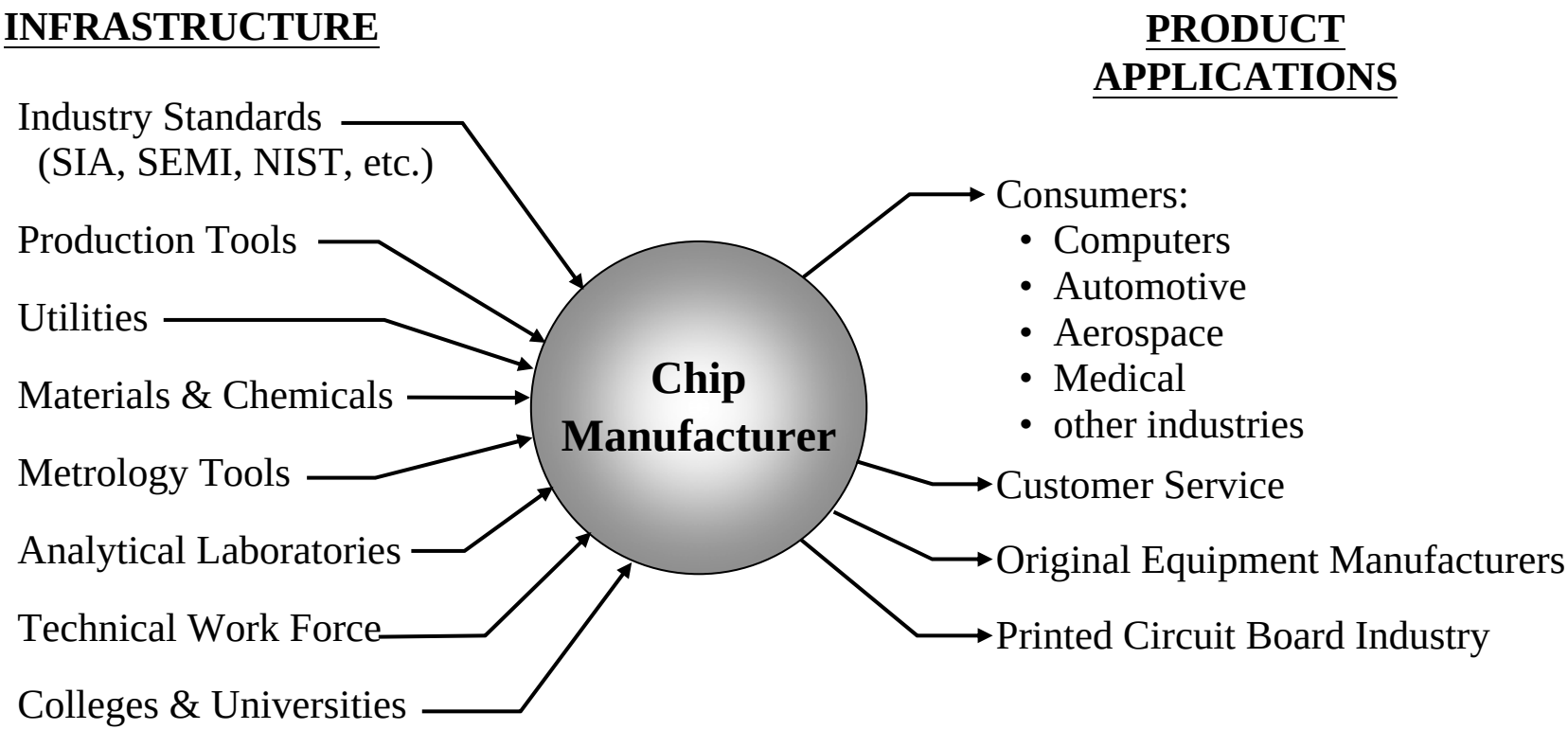
Chapter 1
Introduction to The Semiconductor Industry

The Semiconductor Industry



Worldwide sales of microchips : > $250 billion in 2005

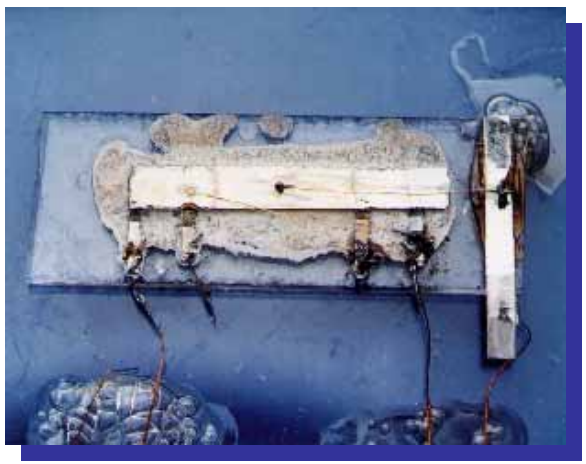
SIA: semiconductor industry association

From Devices to Integrated Circuits

(1947) The First Solid-state Transistor

Lucent Technologies, Bell Labs Innovations, William Shockley, John Bardeen, Walter Brattain (1956 Nobel Prize in physics)

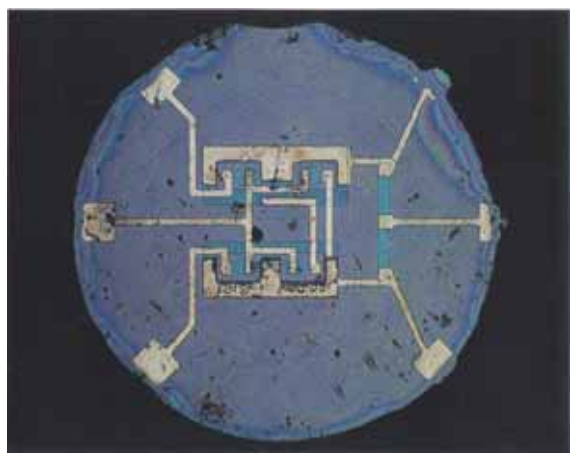
(1958) The First Integrated Circuit (IC) Device - Oscillator IC (5 components)



Texas Instruments, Inc., Jack Kilby

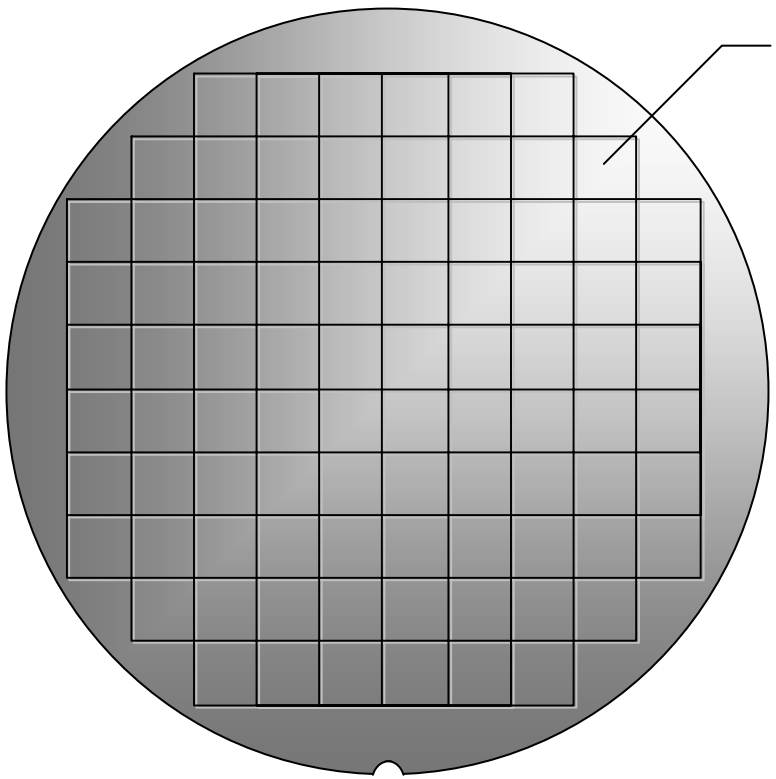
- **1950s: Transistor Technology**
- **1960s: Process Technology**
- **1970s: Competition**
- **1980s: Automation**
- **1990s: Volume Production**

(1961) The First Planar IC (Transistor+R+C)



Fairchild Semiconductor, California (Silicon Valley), Robert Noyce

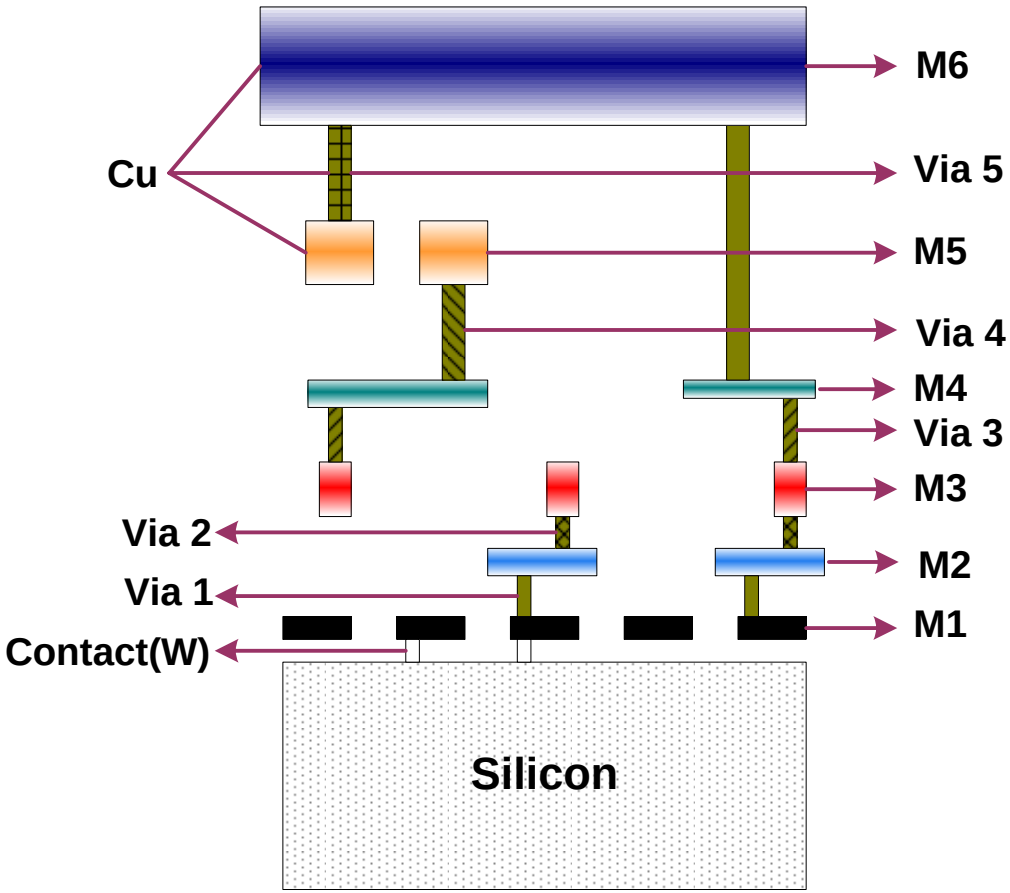
Top View of Wafer with Chips

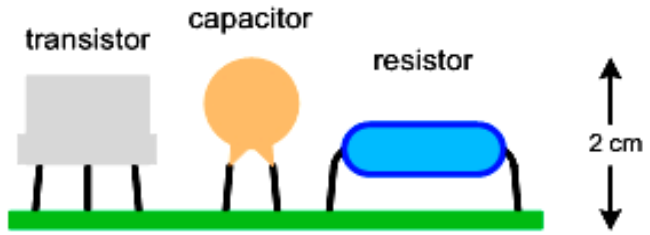


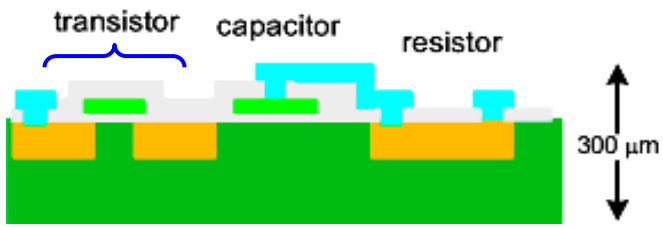
A single integrated circuit, also known as a die, chip, and microchip

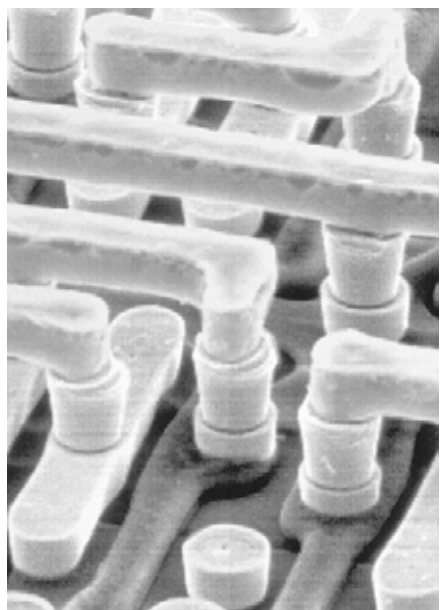
Snapshot- Profile of IC

8 metal layers – over the past 25 years







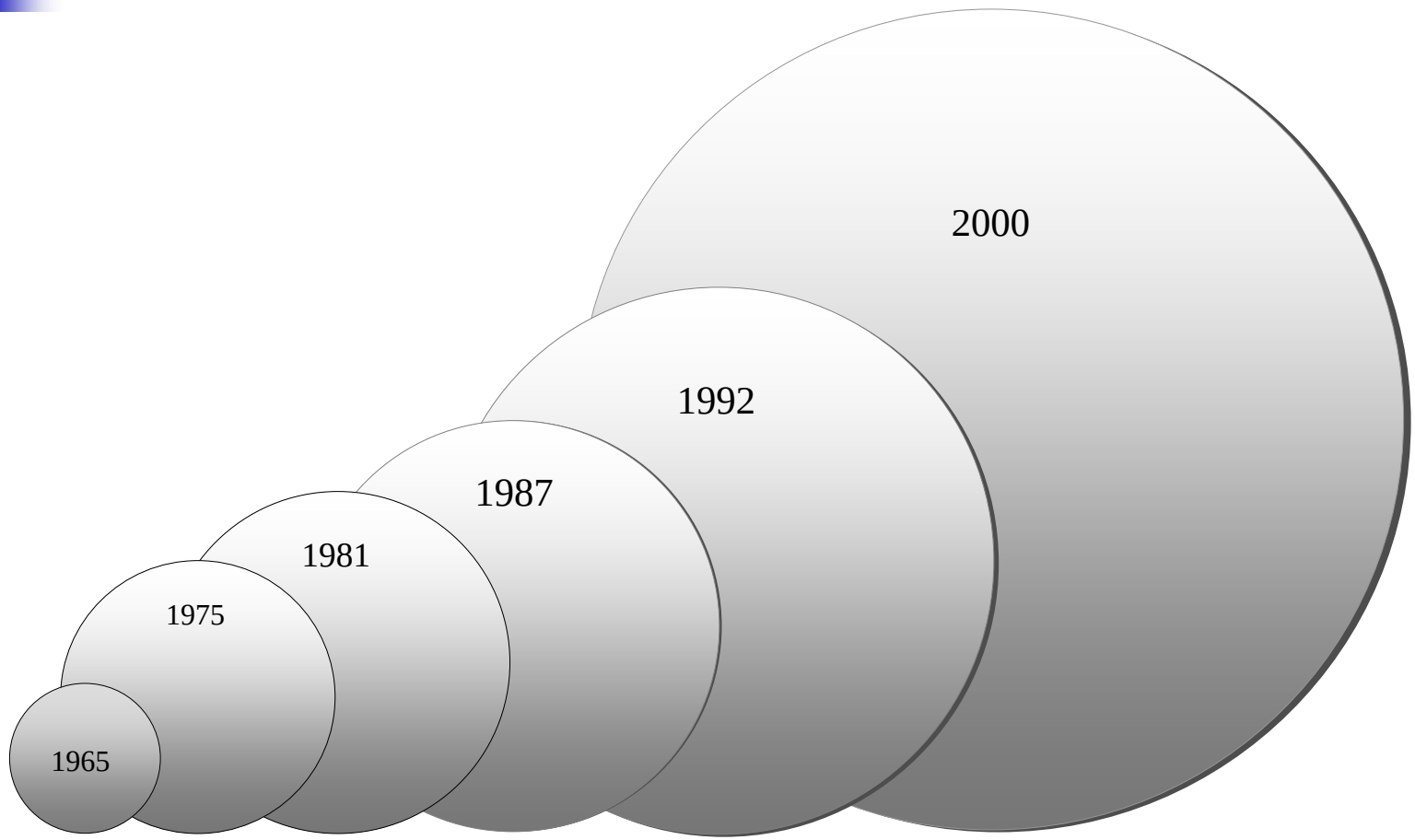


2005 VLSI TECH.
中山電機 黃義佑

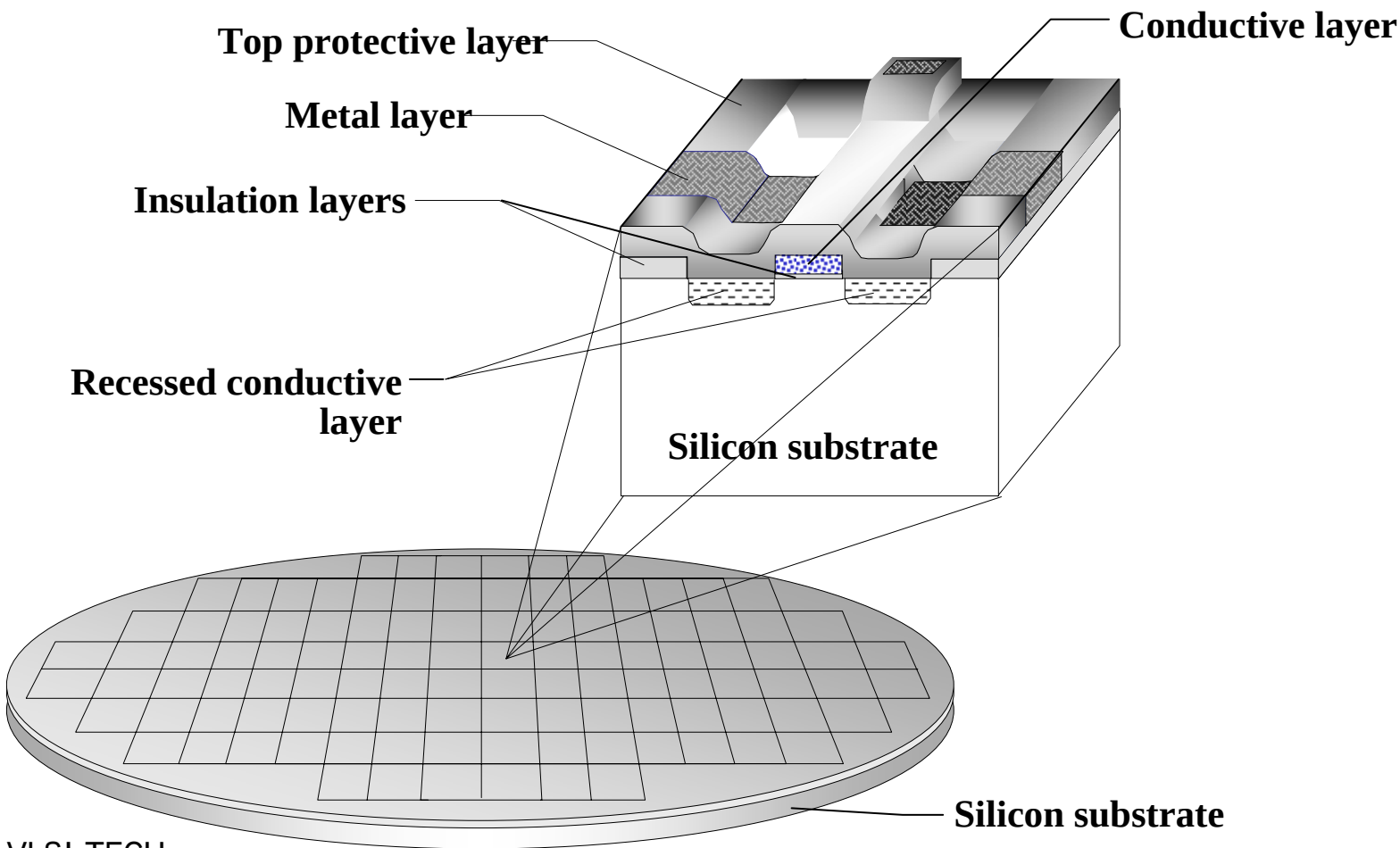
IC Fabrication

- Silicon
  - Wafer
  - Wafer Sizes
  - Devices and Layers
- Wafer Fab
- Stages of IC Fabrication
  - Wafer preparation
  - Wafer fabrication
  - Wafer test/sort
  - Assembly and packaging
  - Final test

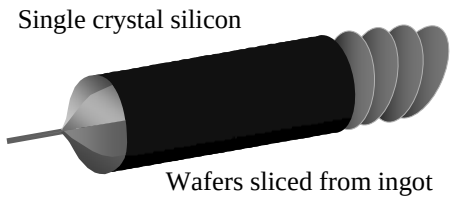
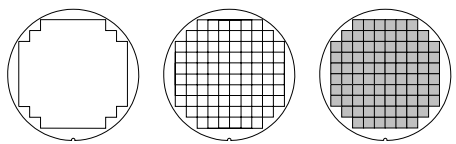
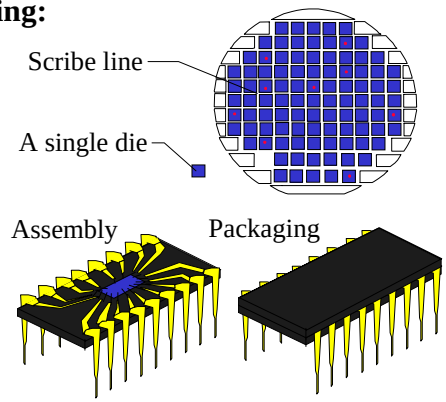
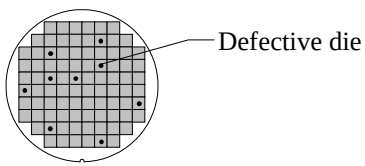
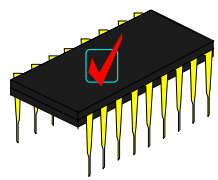
Evolution of Wafer Size



Devices and Layers from a Silicon Chip

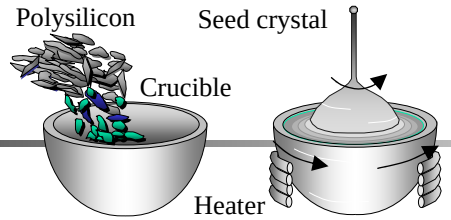


Stages of IC Fabrication

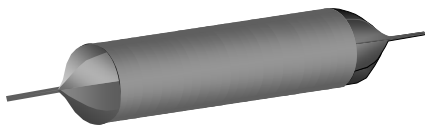
1.	**Wafer Preparation** includes crystal growing, rounding, slicing and polishing.		4.	**Assembly and Packaging:** The wafer is cut along scribe lines to separate each die. Metal connections are made and the chip is encapsulated.
2.	**Wafer Fabrication** includes cleaning, layering, patterning, etching and doping.			
3.	**Test/Sort** includes probing, testing and sorting of each die on the wafer.		5.	**Final Test** ensures IC passes electrical and environmental testing.
				

Preparation of Silicon Wafers

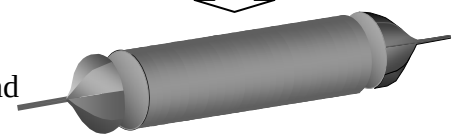
1. Crystal Growth



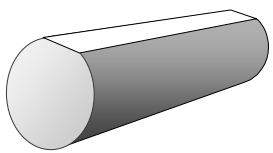
2. Single Crystal Ingot



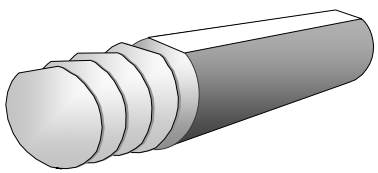
3. Crystal Trimming and Diameter Grind



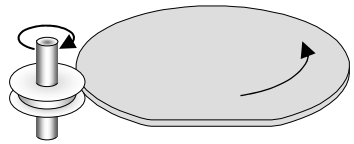
4. Flat Grinding



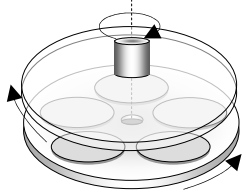
5. Wafer Slicing



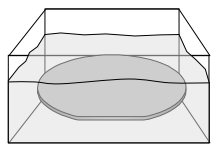
6. Edge Rounding



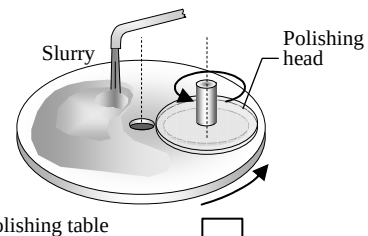
7. Lapping



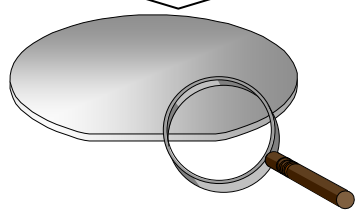
8. Wafer Etching



9. Polishong



10. Wafer Inspection

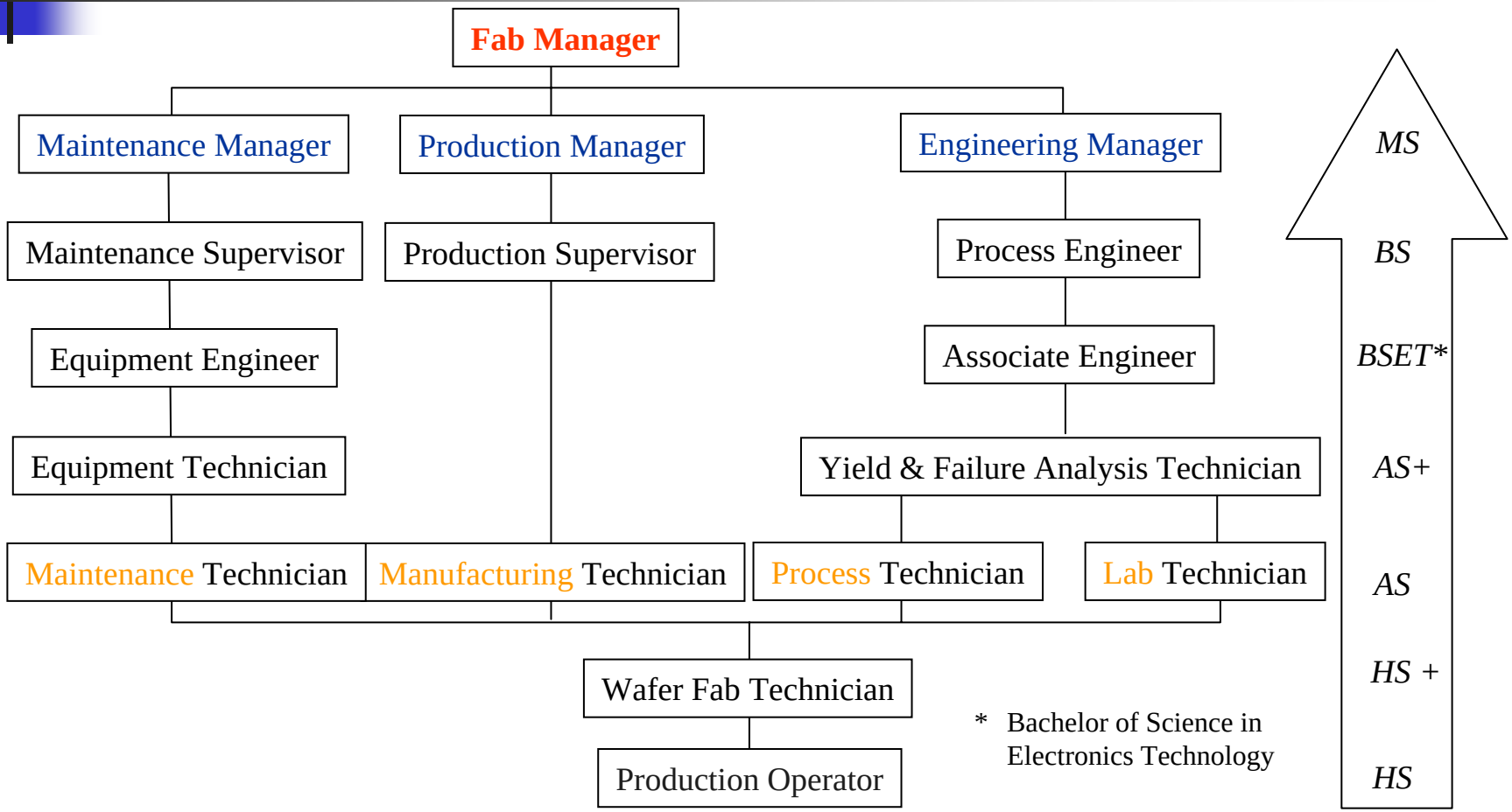


(*Note:* Terms in Figure 1.7 are explained in Chapter 4.)

Wafer Fab

2005 VLSI TECH. Photo courtesy of Advanced Micro Devices-Dresden, © S. Doering

Career Paths in the Semiconductor Industry



Circuit Integration of Semiconductors - Integration Eras

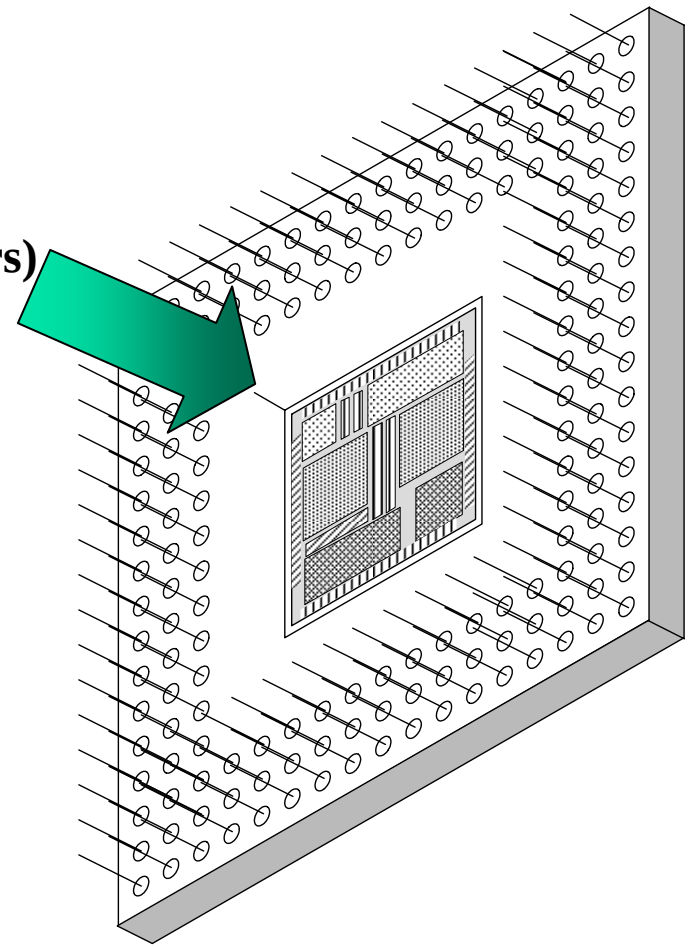
Circuit Integration	Semiconductor Industry Time Period	Number of Components per Chip
No integration (discrete components)	Prior to 1960	1
Small scale integration (SSI)	Early 1960s	2 to 50
Medium scale integration (MSI)	1960s to Early 1970s	50 to 5,000
Large scale integration (LSI)	Early 1970s to Late 1970s	5,000 to 100,000
Very large scale integration (VLSI)	Late 1970s to Late 1980s	100,000 to 1,000,000
Ultra large scale integration (ULSI)	1990s to present	> 1,000,000

Semiconductor Trends :

- **Increase in Chip Performance**
  - **–Components per Chip** ↑
  - **–Power Consumption** ↓
- **Increase in Chip Reliability**
- **Reduction in Chip Price**

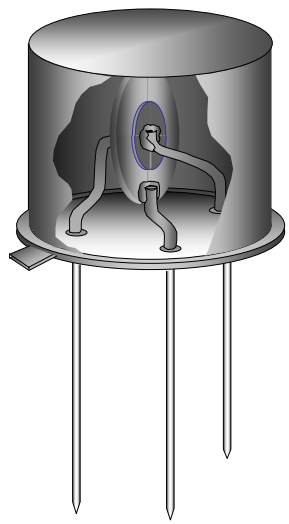
Size Comparison of Early and Modern Semiconductors

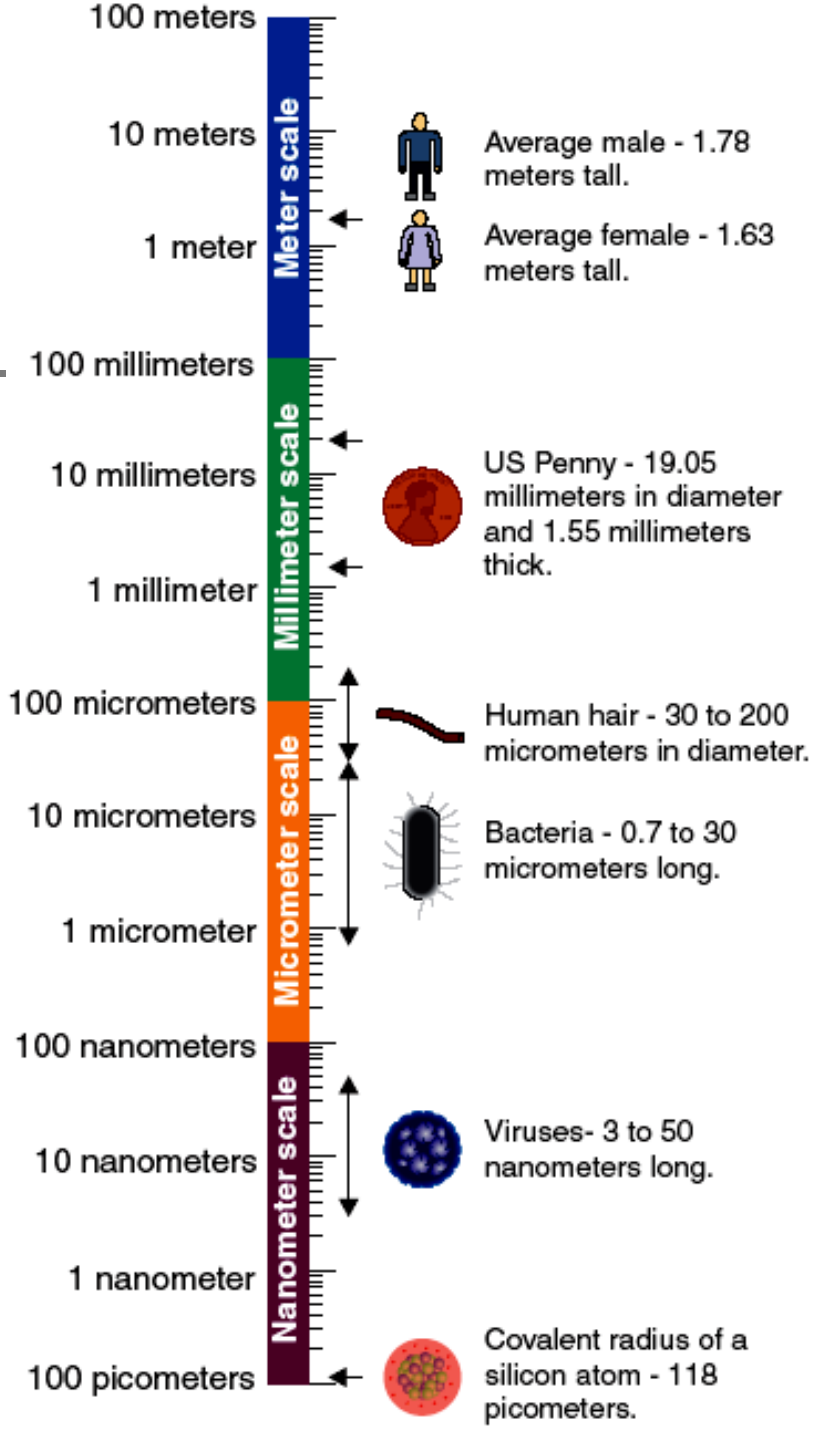
1990s Microchip
(5~25 million transistors)



U.S. coin, 10 cents

1960s Transistor

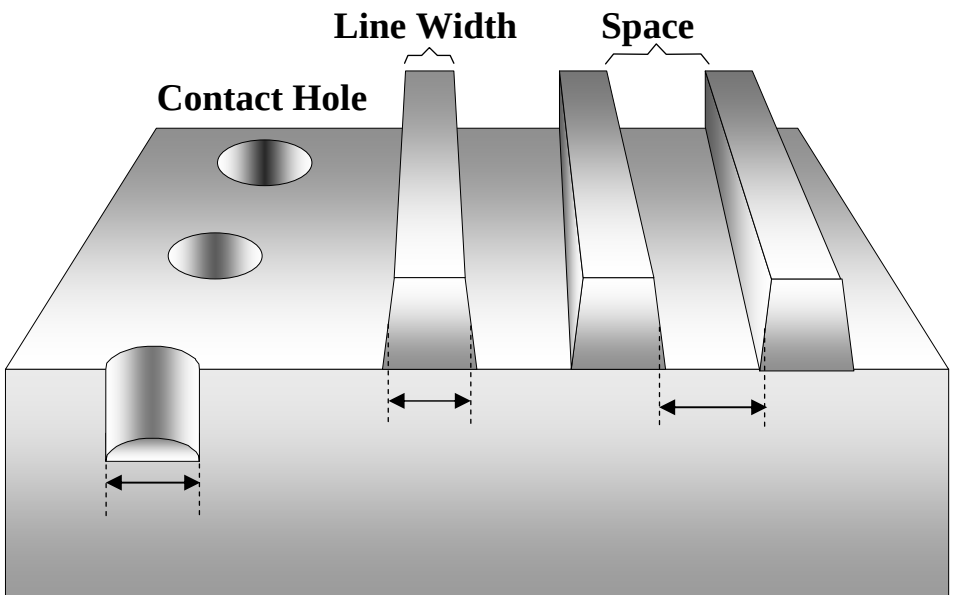



100 meters
10 meters
1 meter
100 millimeters
10 millimeters
1 millimeter
100 micrometers
10 micrometers
1 micrometer
100 nanometers
10 nanometers
1 nanometer
100 picometers
Meter scale
Millimeter scale
Micrometer scale
Nanometer scale
Average male - 1.78 meters tall.
Average female - 1.63 meters tall.
US Penny - 19.05 millimeters in diameter and 1.55 millimeters thick.
Human hair - 30 to 200 micrometers in diameter.
Bacteria - 0.7 to 30 micrometers long.
Viruses- 3 to 50 nanometers long.
Covalent radius of a silicon atom - 118 picometers.

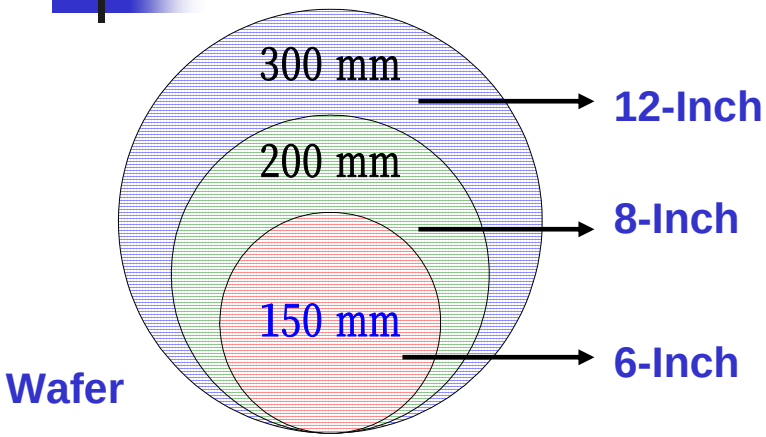
Past and Future Technology Nodes for Device Critical Dimension (CD)

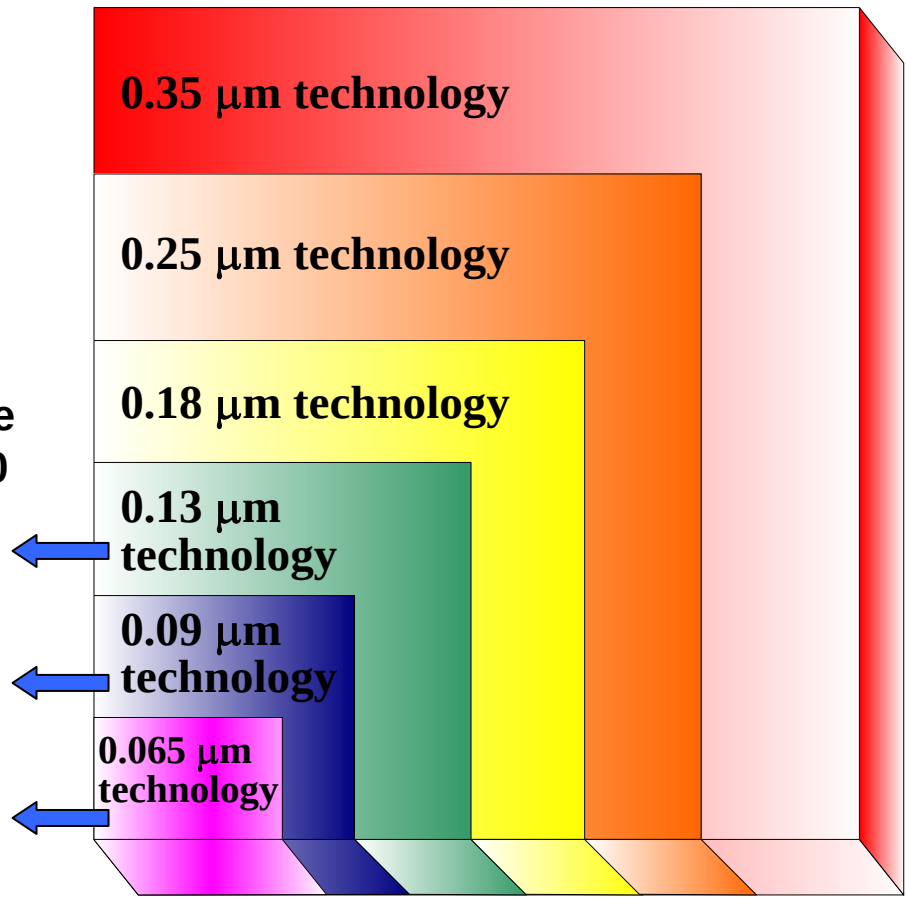
	1988	1992	1995	1997	1999	2001	2002	2005
CD (μm)	1.0	0.5	0.35	0.25	0.18	0.15	0.13	0.10

Common IC Features



Feature Technology and Size





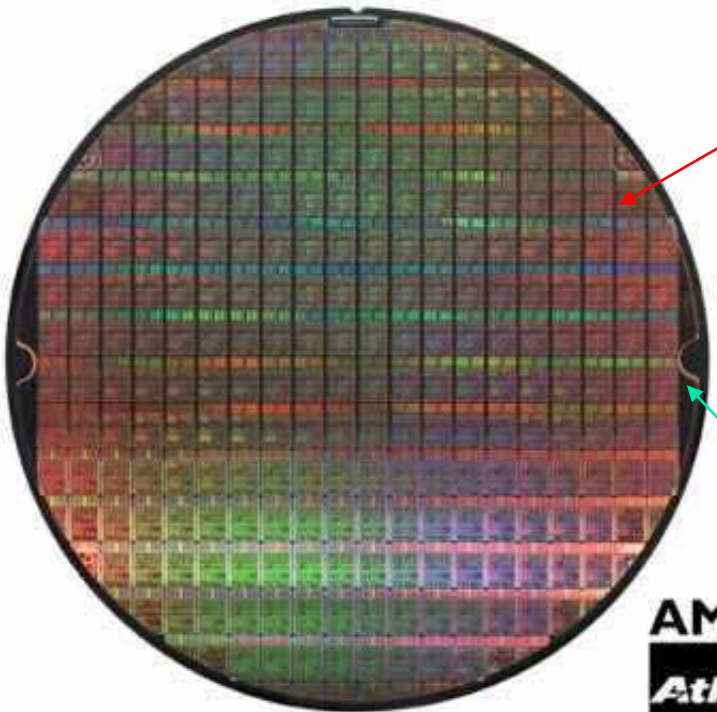
When compared to the 0.18-micron process, the new 0.13-micron process results in less than 60 percent the die size and nearly 70 percent improvement in performance

The 90-nm process will be manufactured on 300mm wafers

NEC devises low-k film for second-generation 65-nm process

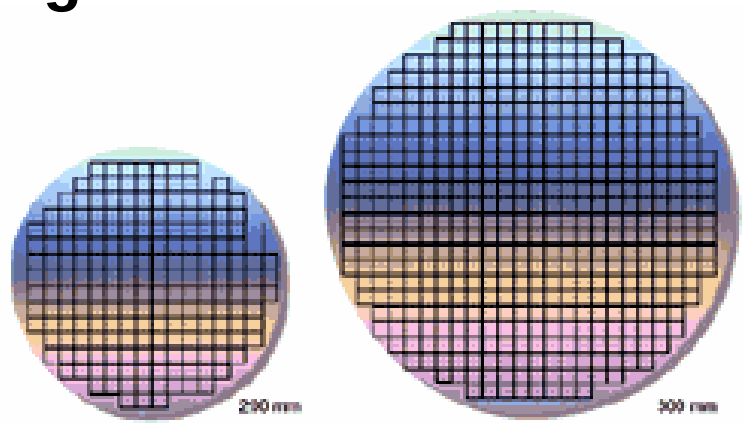
Die Size

- **Wafer photo**



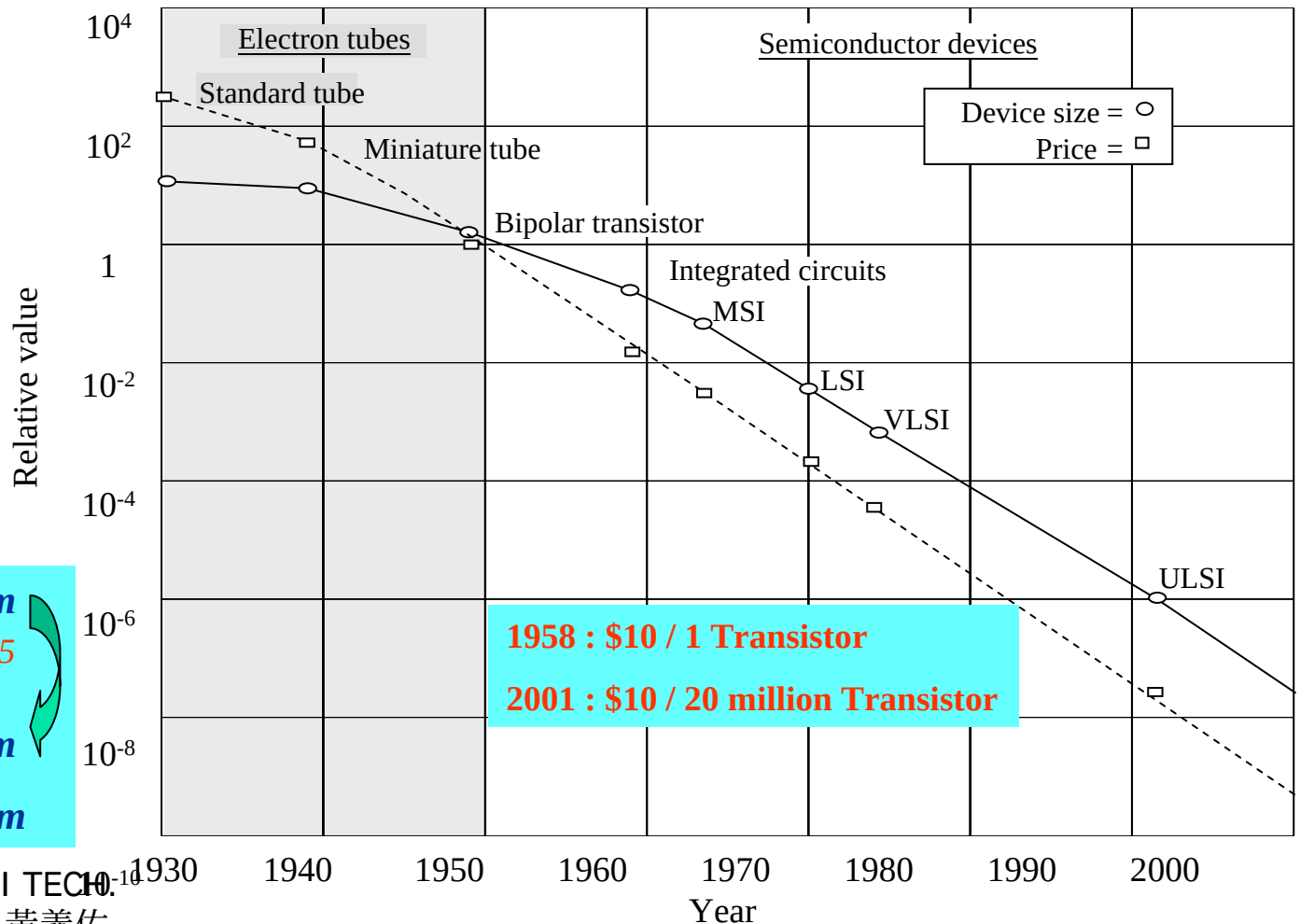
Single die

Wafer



From http://www.amd.com

Price Decrease of Semiconductor Chips



1995 : CD=0.35 μm

increase 150~275 chips per wafer

1997 : CD=0.25 μm

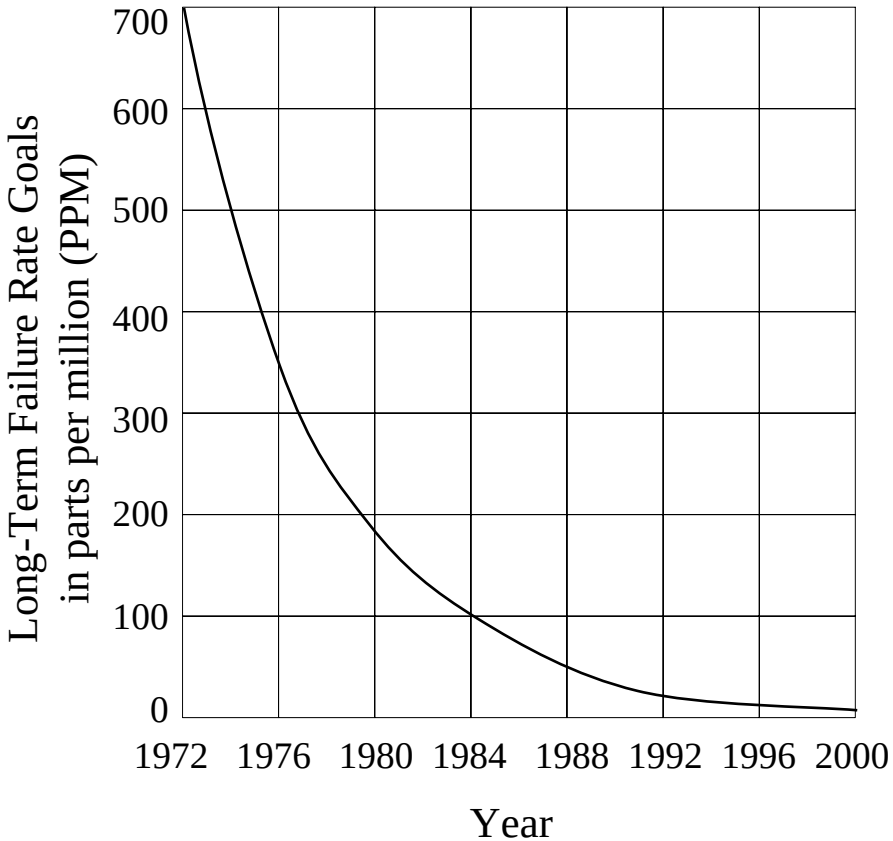
2002 : CD=0.13 μ m

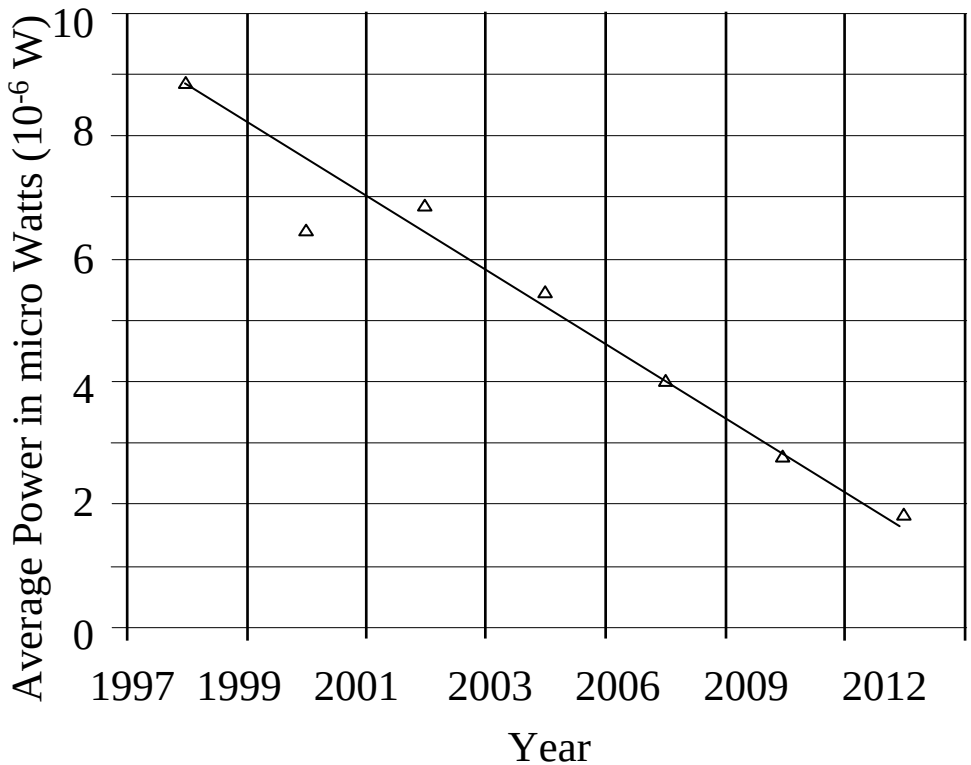
1958 : $10 / 1 Transistor

2001 : $10 / 20 million Transistor

Redrawn from C. Chang & S. Sze, McGraw-Hill, *ULSI Technology*, (New York: McGraw-Hill, 1996), xxiii.

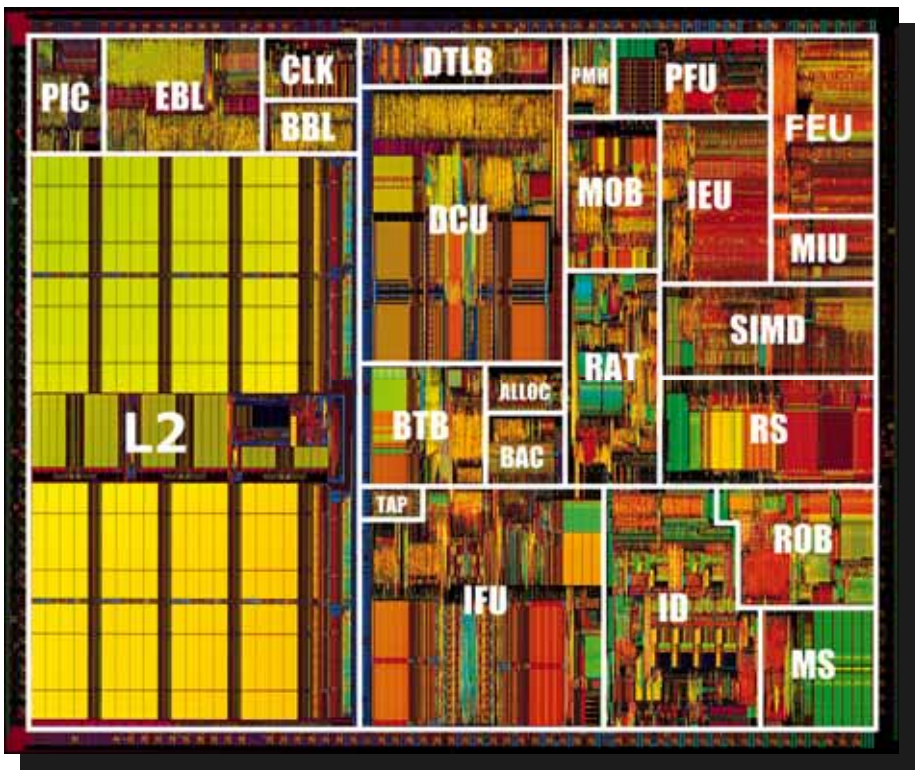
Reliability Improvement of Chips & Reduction in Chip Power Consumption per IC



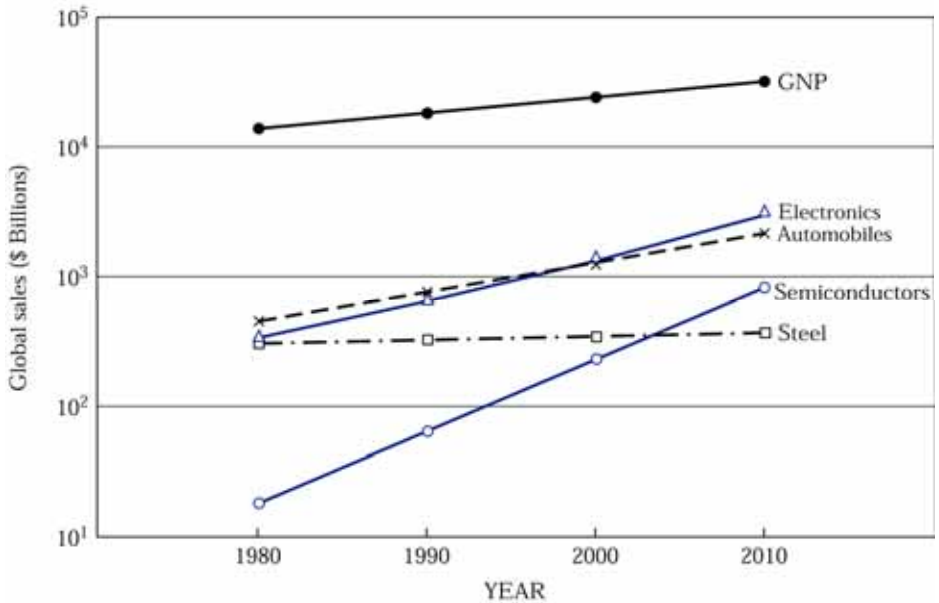


Redrawn from Semiconductor Industry Association (SIA)
National Technology Roadmap, 1997

ULSI Chip



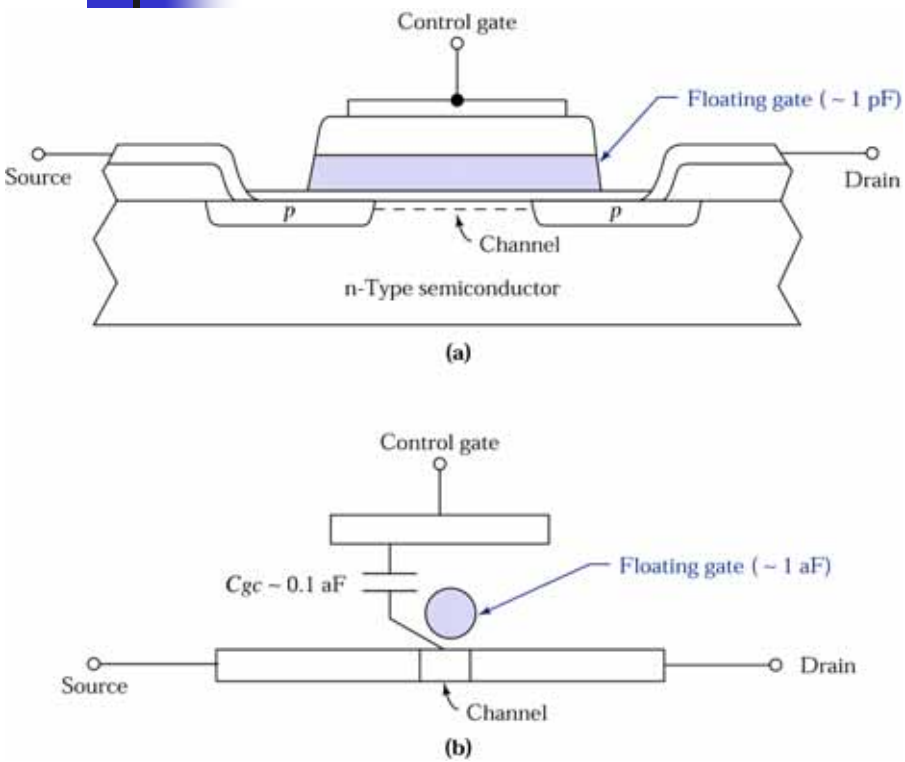
Intel Corporation, Pentium III



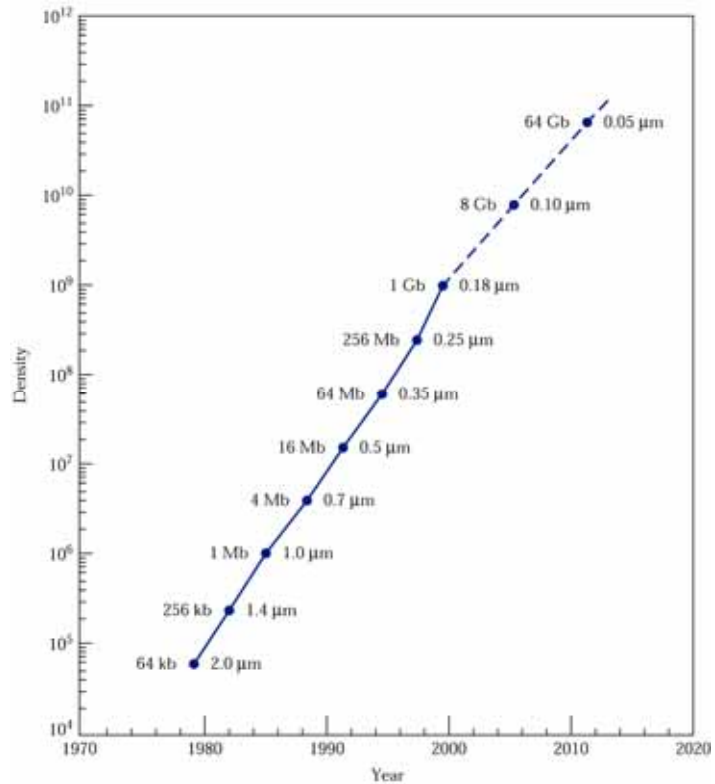
▸ **Gross world product (GWP) and sales volumes of the electronics, automobile, semiconductor, and steel industries from 1980 to 2000 and projected to 2010.**

IC Product #1:

Semiconductor Memory Devices



▸ (*a*) A schematic diagram of the first nonvolatile semiconductor memory (NVSM) with a floating gate. (*b*) A limiting case of the floating-gate NVSM—the single-electron memory cell.



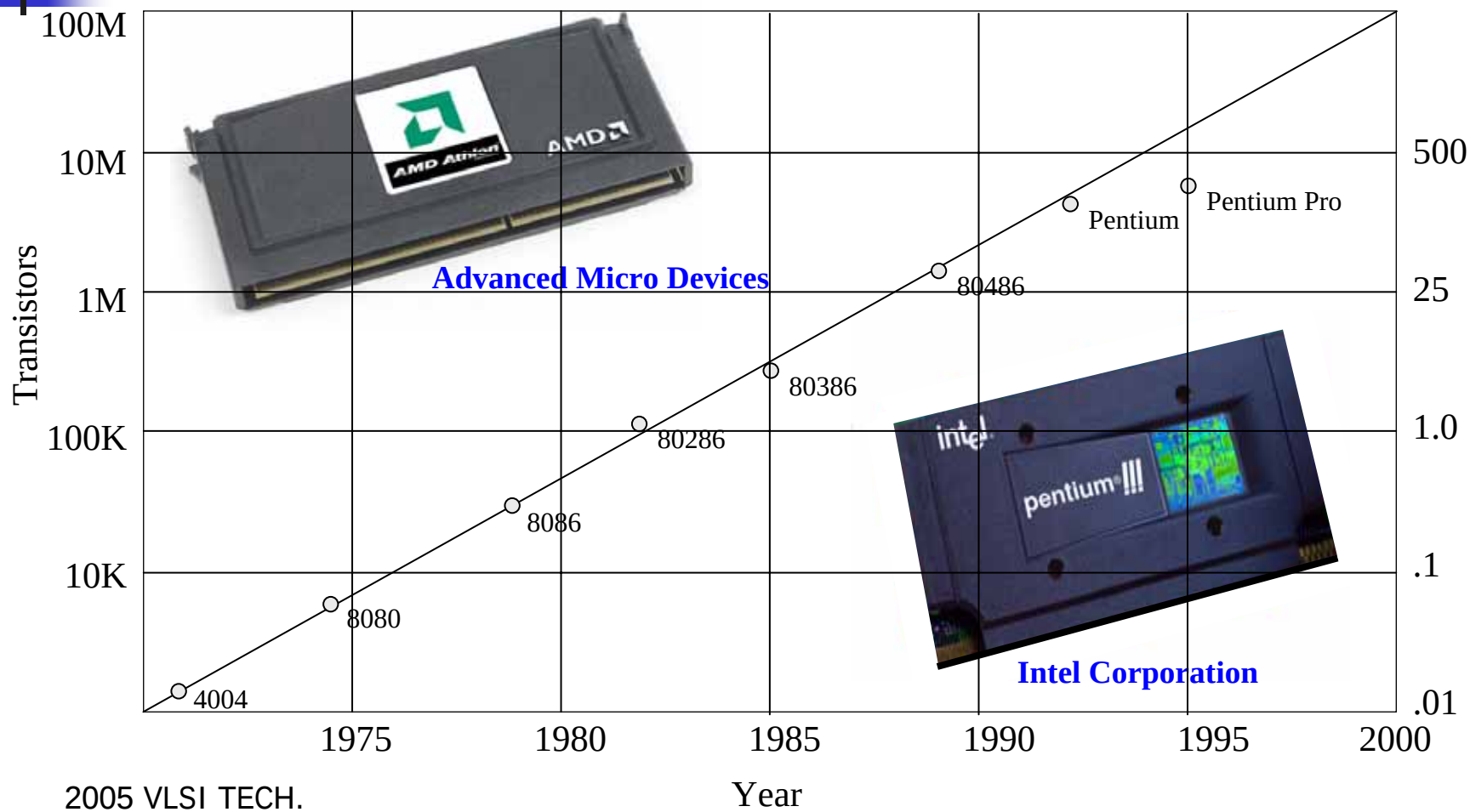
▸ Exponential increase of dynamic random access memory (DRAM) density versus year based on the Semiconductor Industry Association (SIA) roadmap.

NVSM : non-volatility; high device density; low-power consumption; electrical rewritability.

IC Product #2 : Microprocessor Chips

Moore's Law for Microprocessors

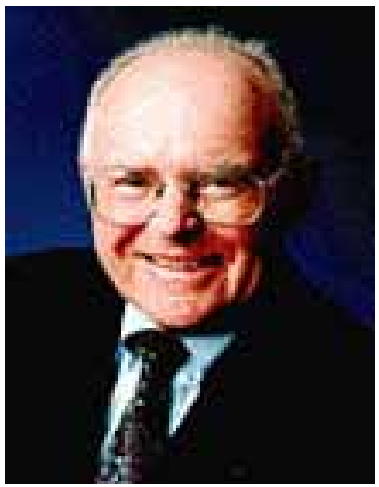
The number of transistors on a chip double every (12) 18 months.



Proceedings of the IEEE, January, 1998, © 1998 IEEE

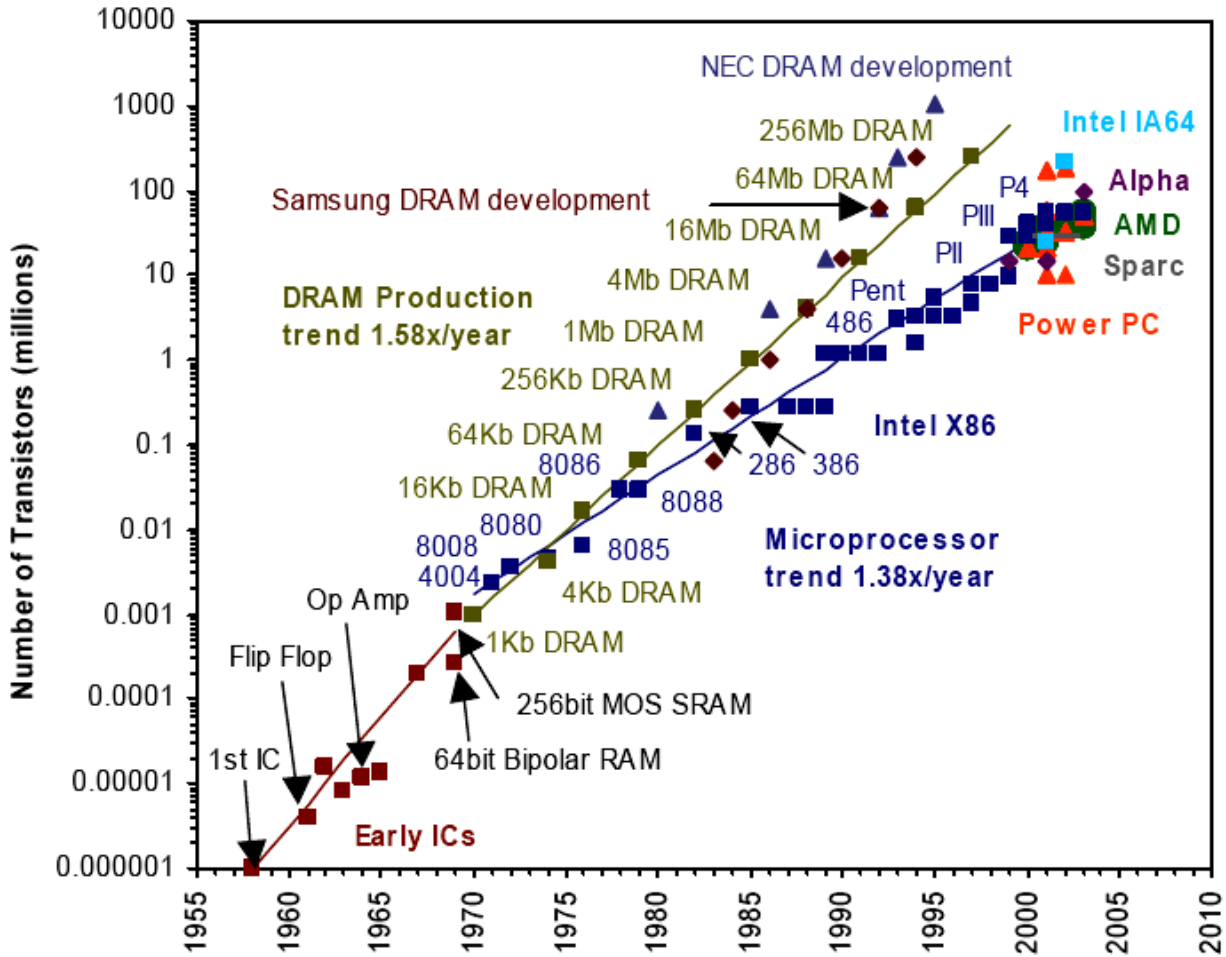
Moore's Law

- **Intel co-founder Gordon Moore notices in 1964**
  - **Number of transistors doubled every 12 months**
  - **Slowed down in the 1980s to every 18 months**
    - Amazingly still correct likely to keep until 2010

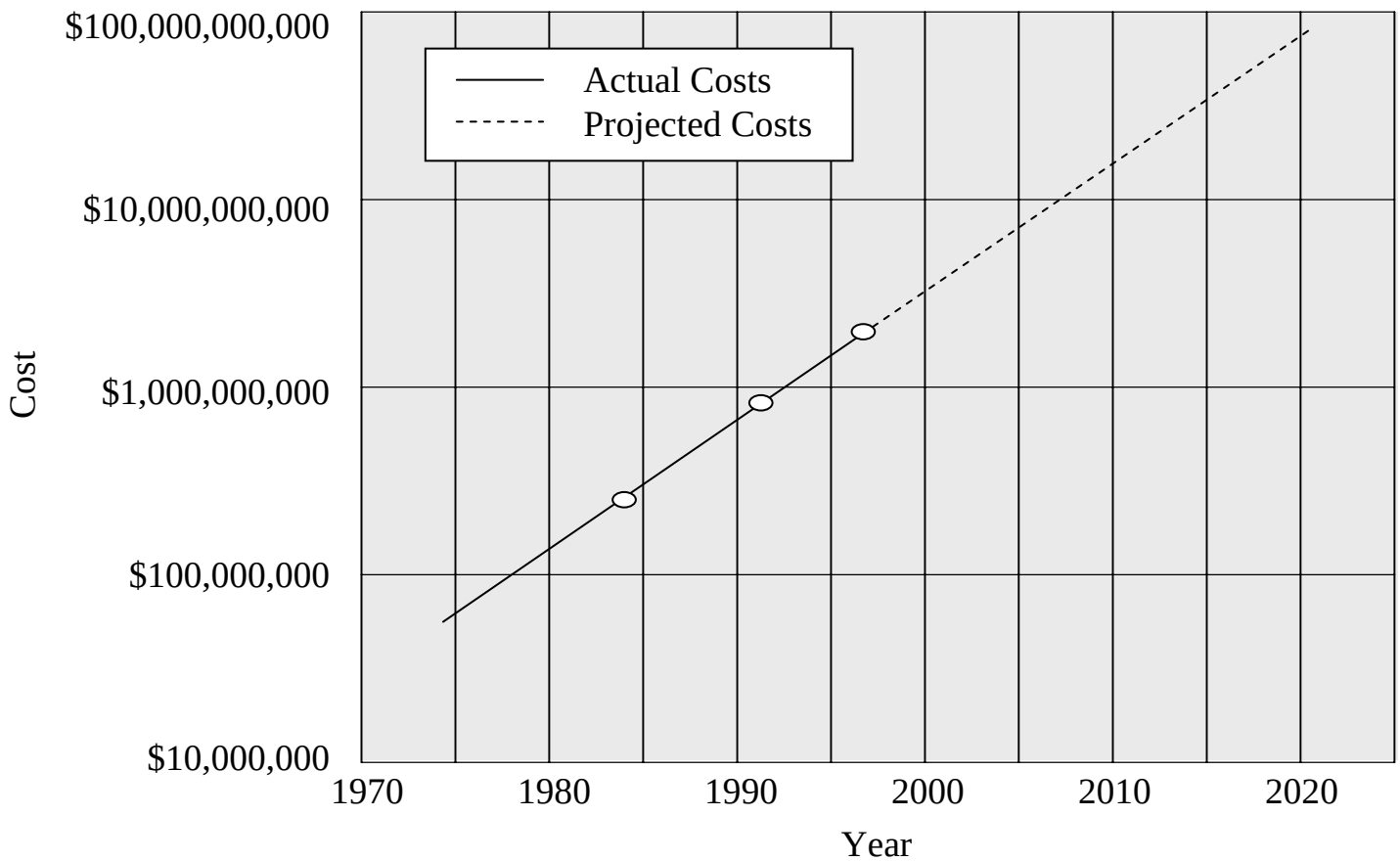


Gordon Moore
Intel Co-Founder and Chairmain Emeritus

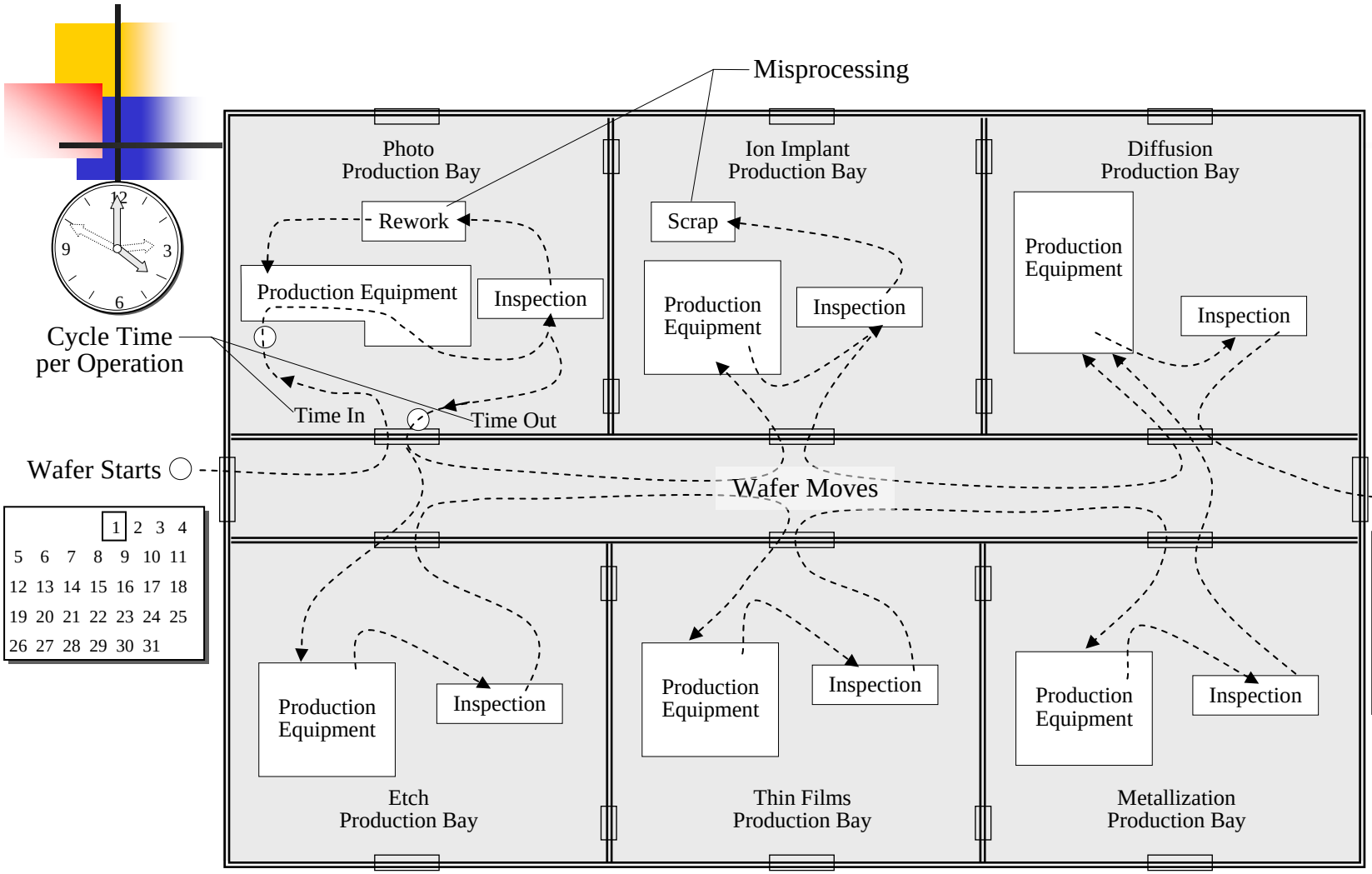
With Moore's Law, IC products can reach low costs, improve performance, and increase the functions.



Start-Up Cost of Wafer Fabs



Productivity Measurements in a Wafer Fab



Production Cycle Time = (Date and Time of Wafer Start) - (Date and Time of Wafer Out)

Wafer Outs = Wafer Starts - Wafers Scrapped

Operator Efficiency = Theoretical Cycle Time / Actual Cycle Time

Equipment Technician in a Wafer Fab

Photograph courtesy of Advanced Micro Devices

Technician in Wafer Fab

Photo courtesy of Advanced Micro Devices