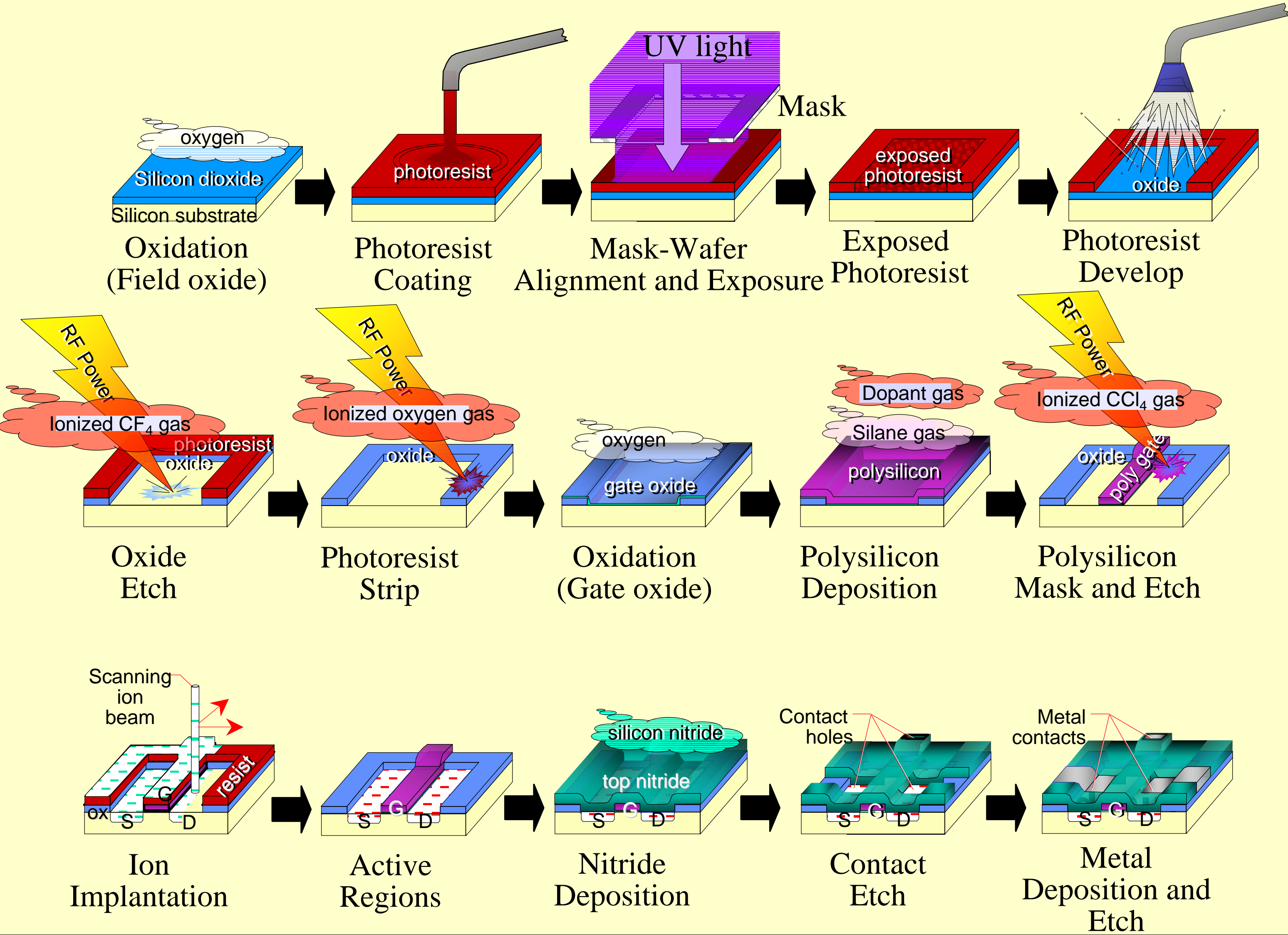
Chapter 4 : ULSI Process Integration
(0.18 μm CMOS Process)

Reference

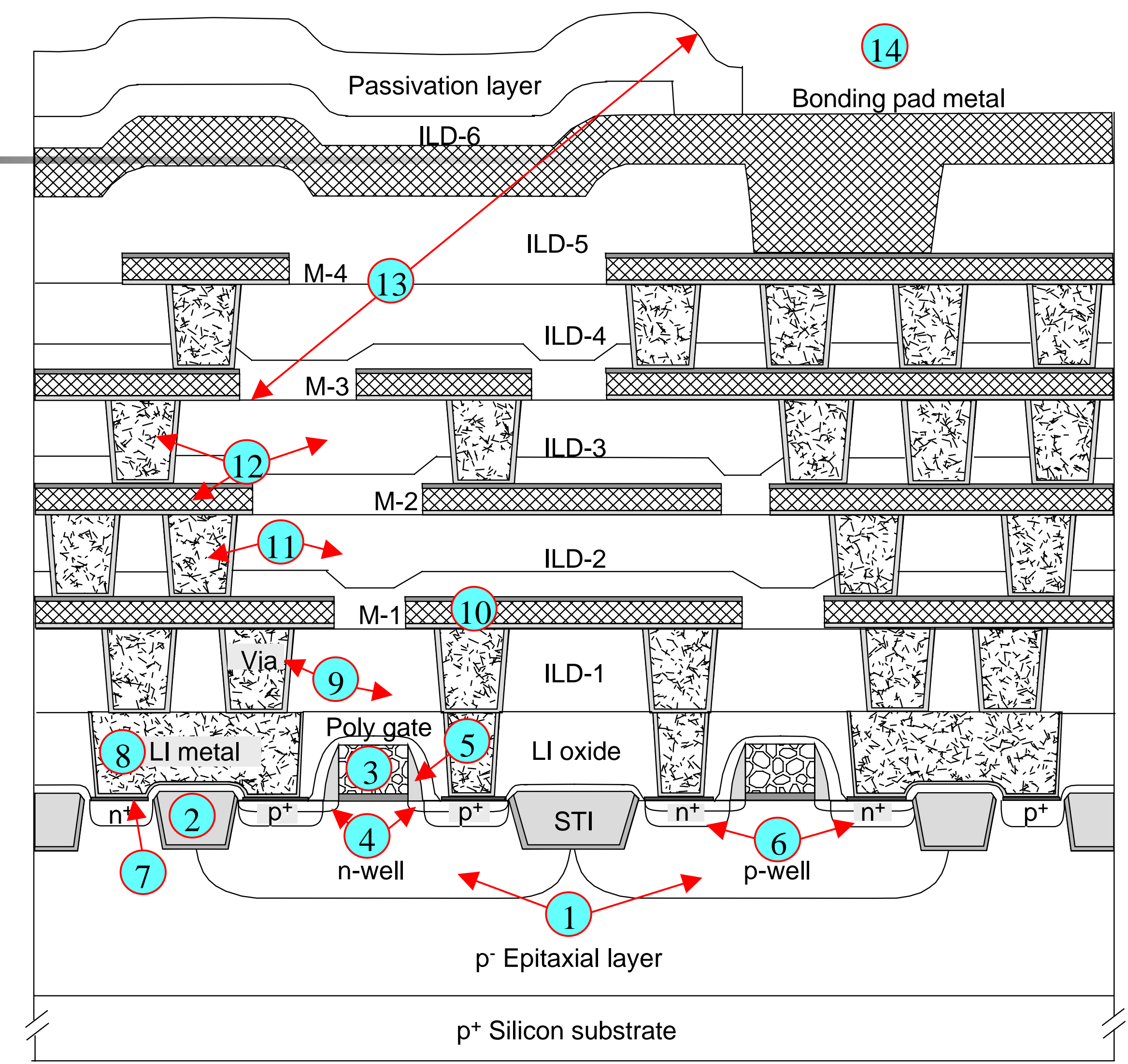
1. **Semiconductor Manufacturing Technology**
   : Michael Quirk and Julian Serda (2001)
2. **國家矽導計畫-教育部晶片法商學程教材 (2004)**
3. **Semiconductor Physics and Devices- Basic Principles(3/e)**
   : Donald A. Neamen (2003)
4. **Semiconductor Devices - Physics and Technology (2/e)**
   : S. M. Sze (2002)
5. **ULSI Technology *: C. Y. Chang, S. M. Sze (1996)***

Major Fabrication Steps in MOS Process Flow

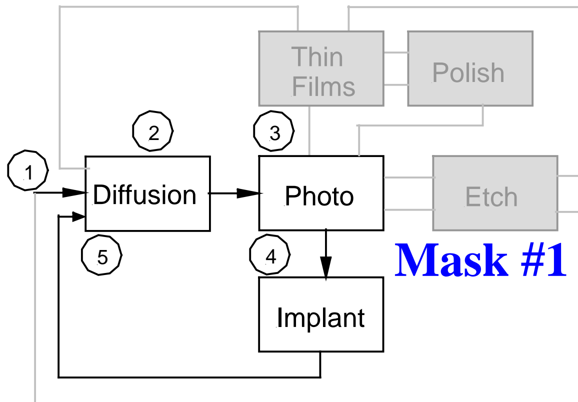


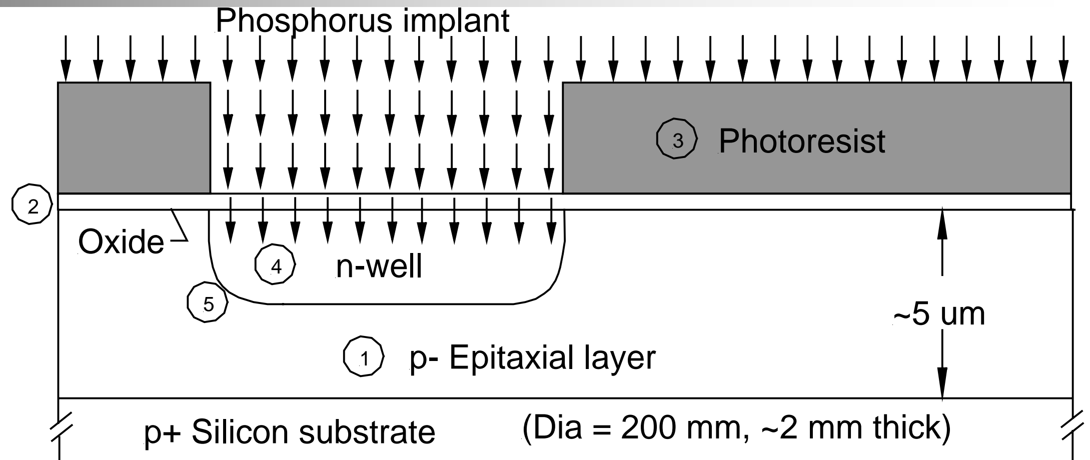
CMOS Manufacturing Steps

1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. LDD Implants
5. Sidewall Spacer
6. S/D Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. Metal-1 Layer
11. ILD-2 to Via-2
12. Metal-2 Layer to Via-3
13. Metal-3 to Pad Etch
14. Parameter Testing

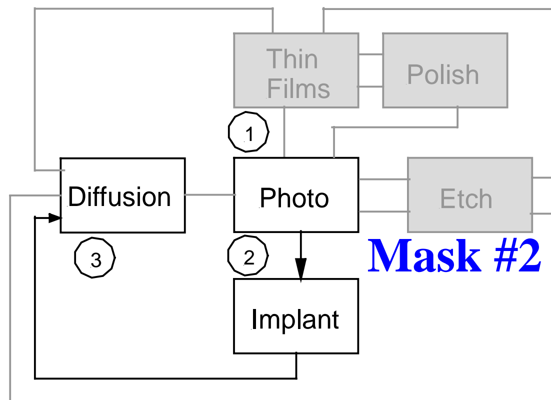


n-well & p-well Formation

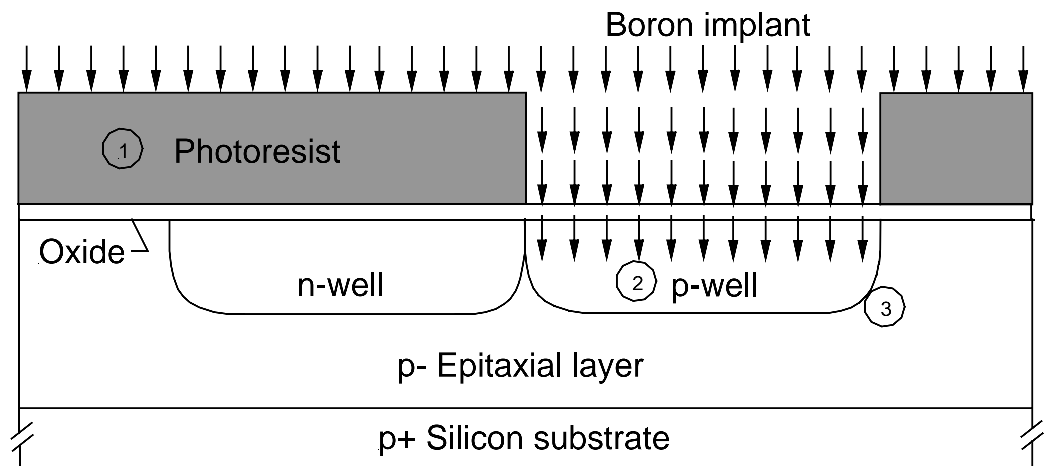




Mask #1



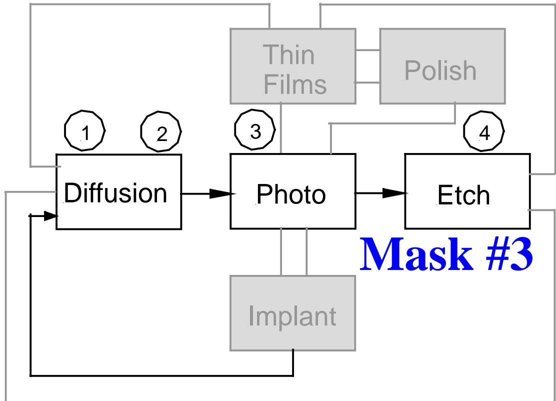
Mask #2

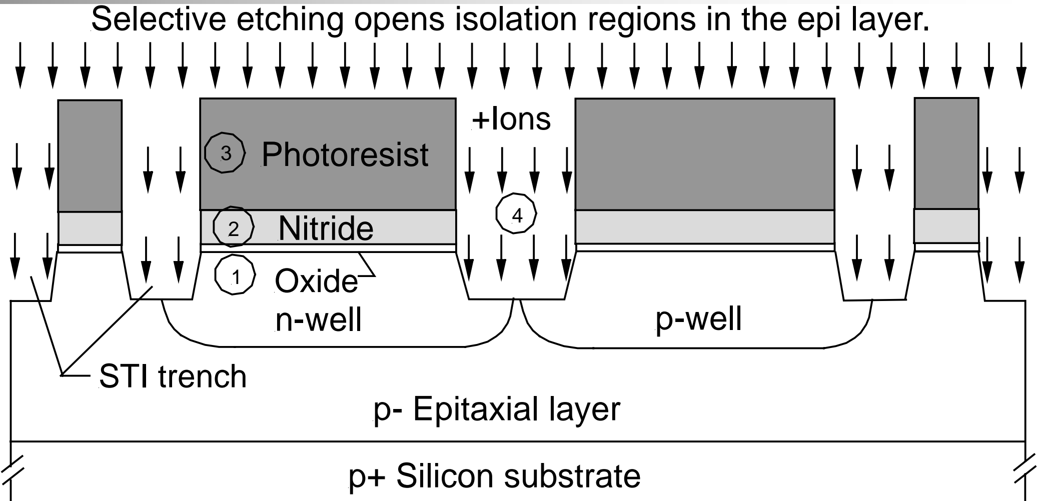


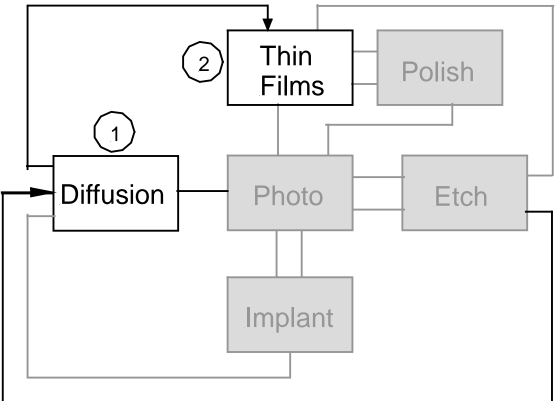
Twin well process

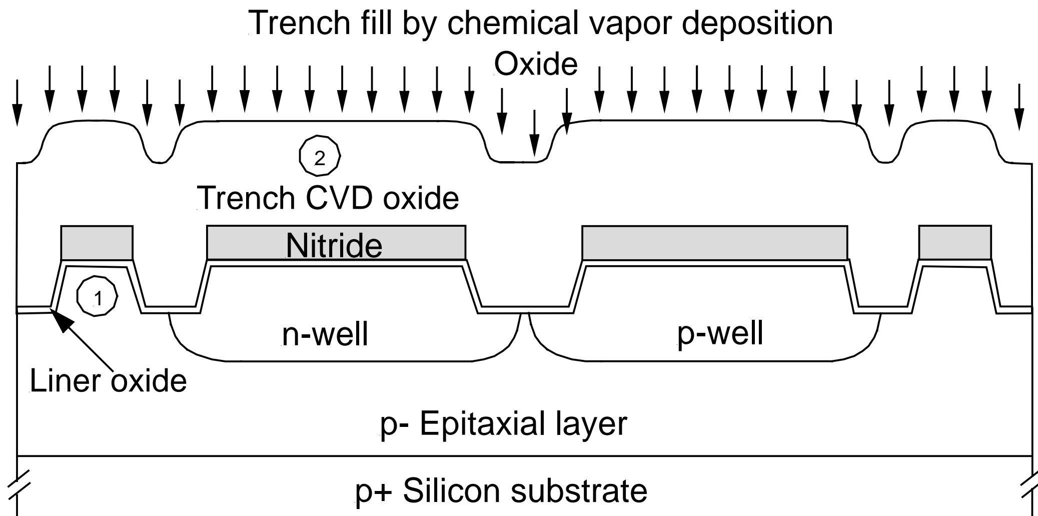
STI Trench Etch & STI Oxide Fill

STI : shallow trench isolation

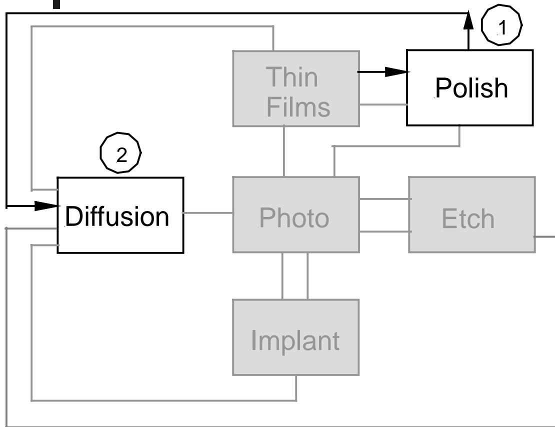


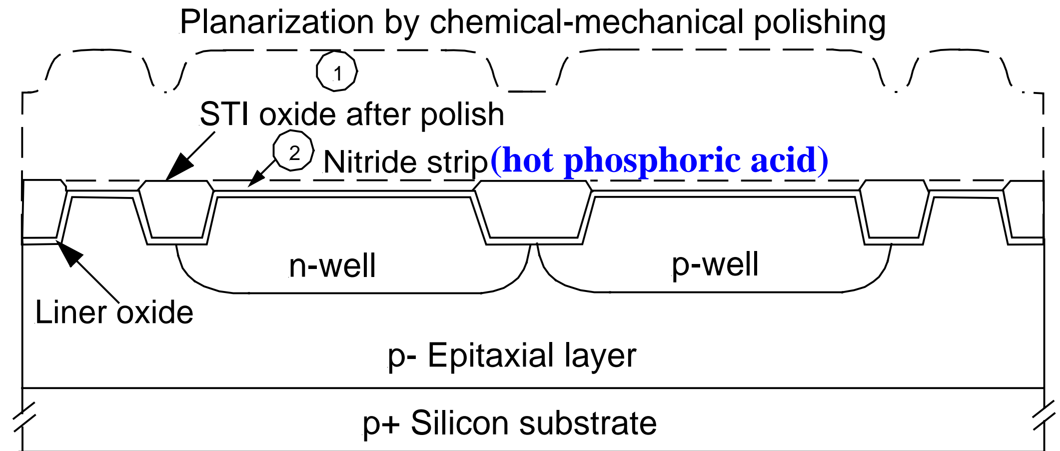


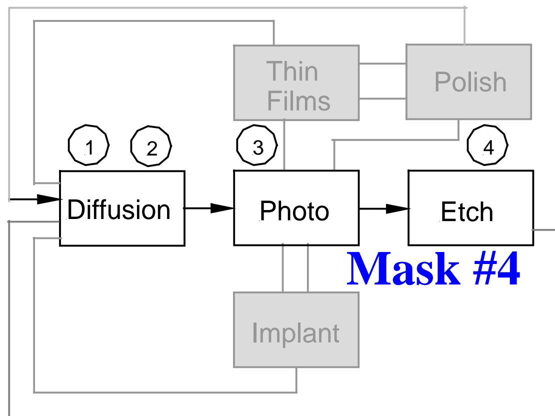


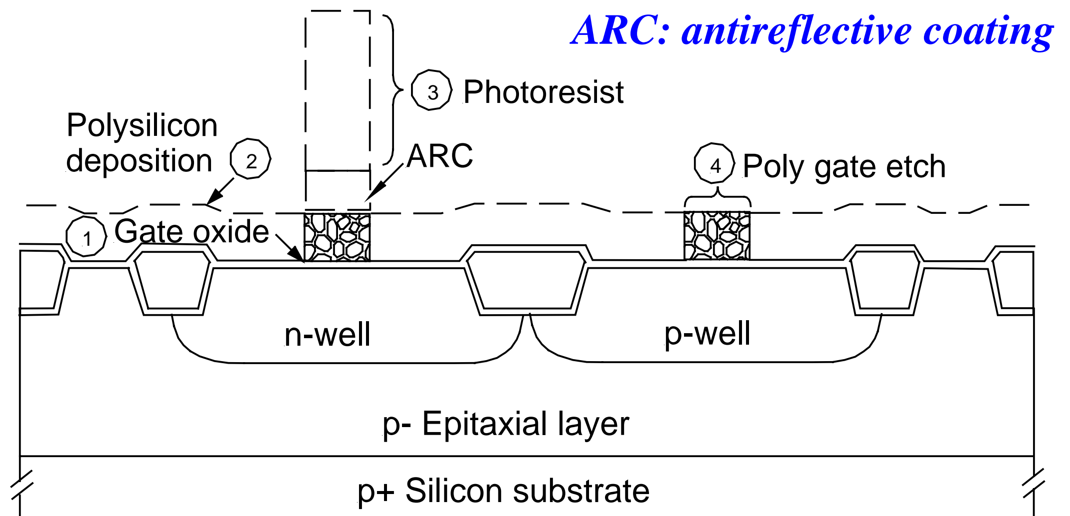


STI Oxide Polish-Nitride Strip & Poly Gate Structure Process



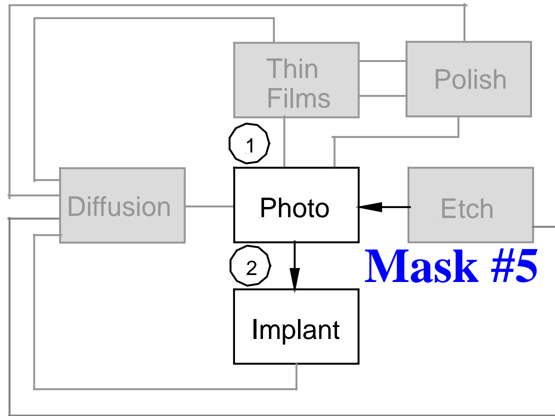


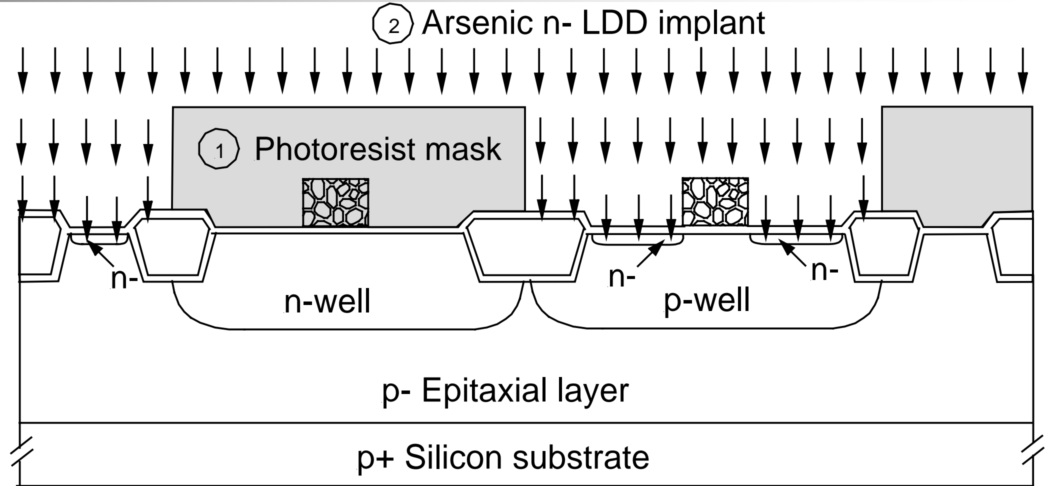




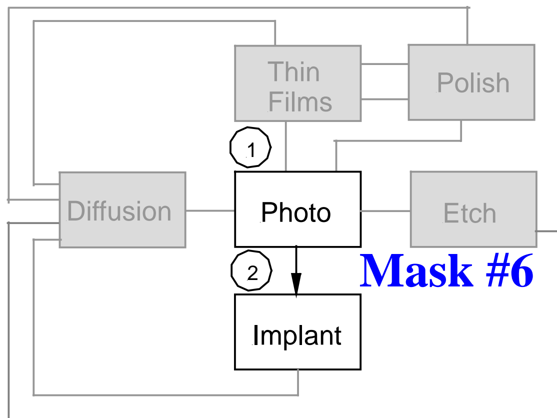
n^- LDD Implant & p^- LDD Implant

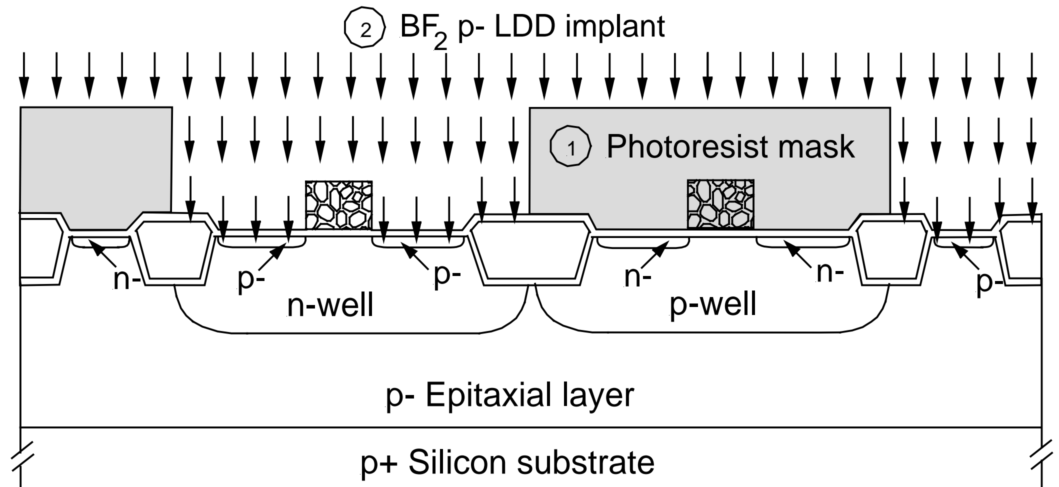
LDD : lightly doped drain





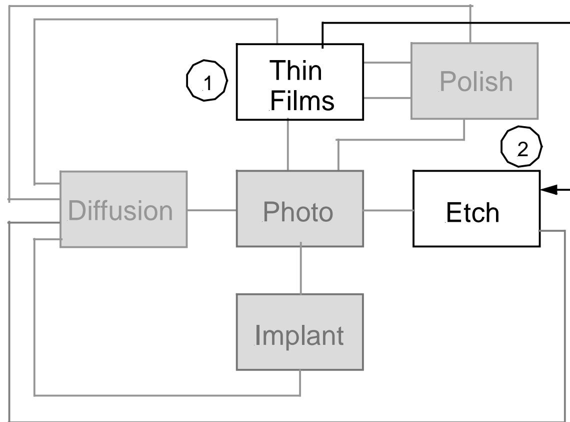
LDD tech. are used to reduce the occurrence of current leakage in channel (due to punchthrough effect)

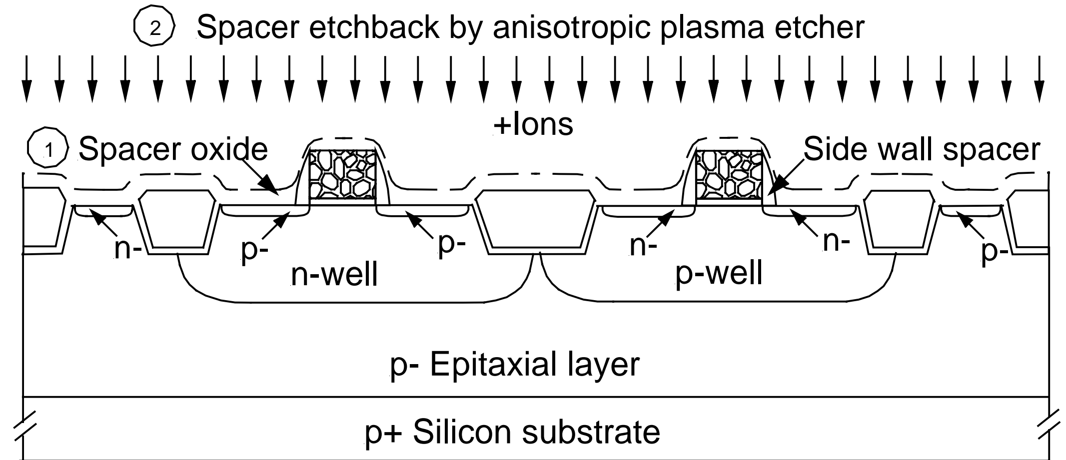




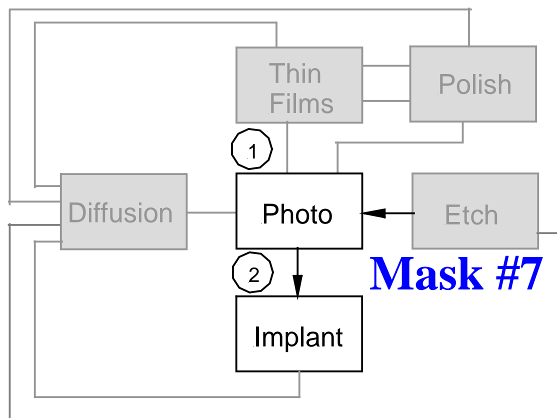
Side Wall Spacer Formation & n+ S/D Implant

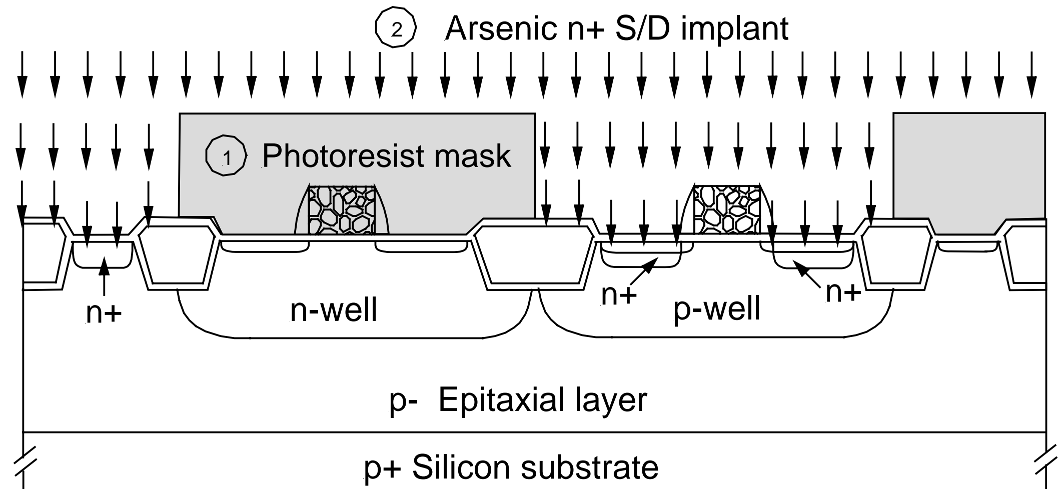
(The dry plasma etcher removes most of the CVD oxide leaving behind the thicker oxide on the sidewalls of the polysilicon gates.)



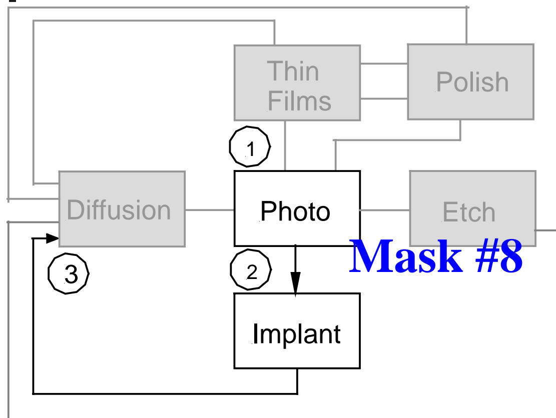


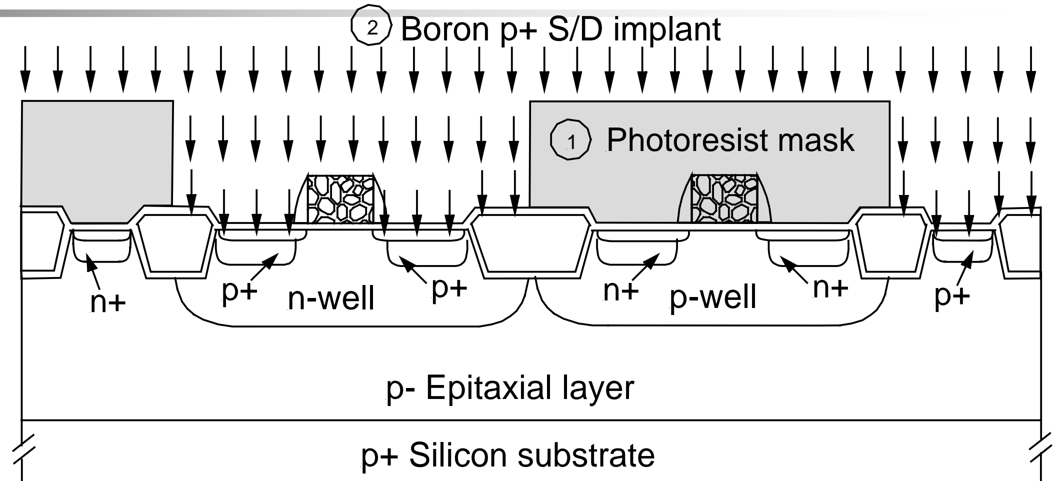
Sidewall spacers will be used alongside the poly gates to prevent the higher S/D implant from penetrating too close to the channel where S/D pumchthrough could occur.

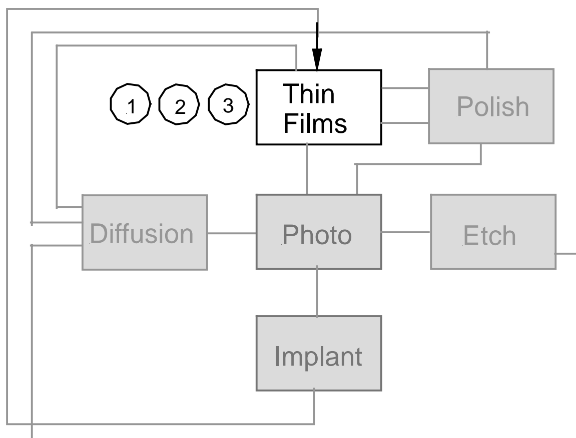


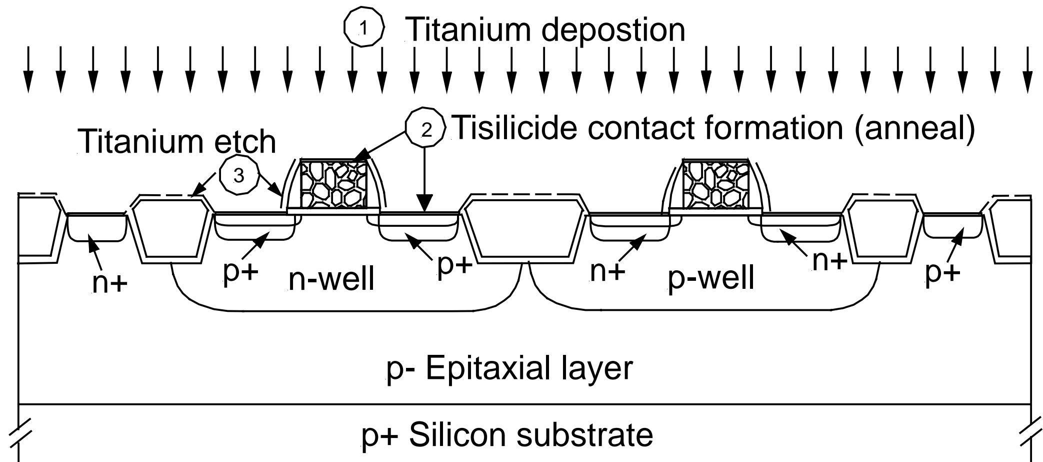


p^+ Source/Drain Implant & Contact Formation



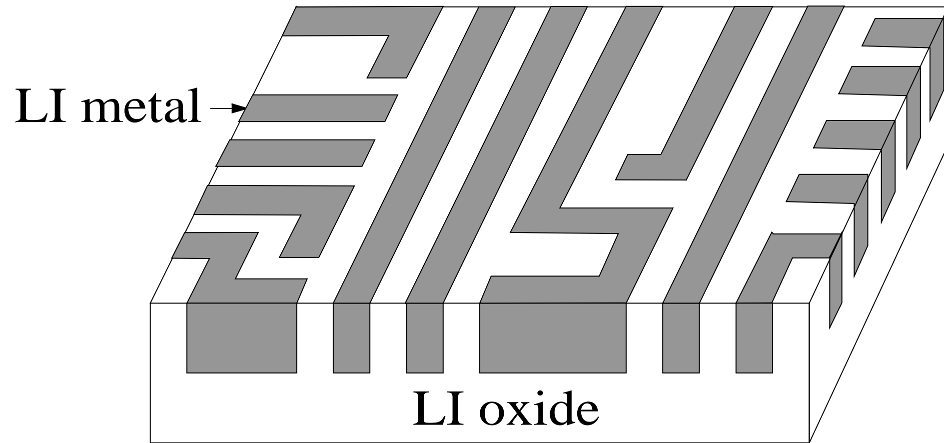




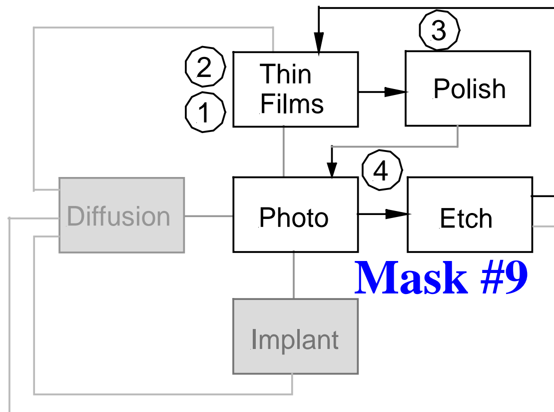


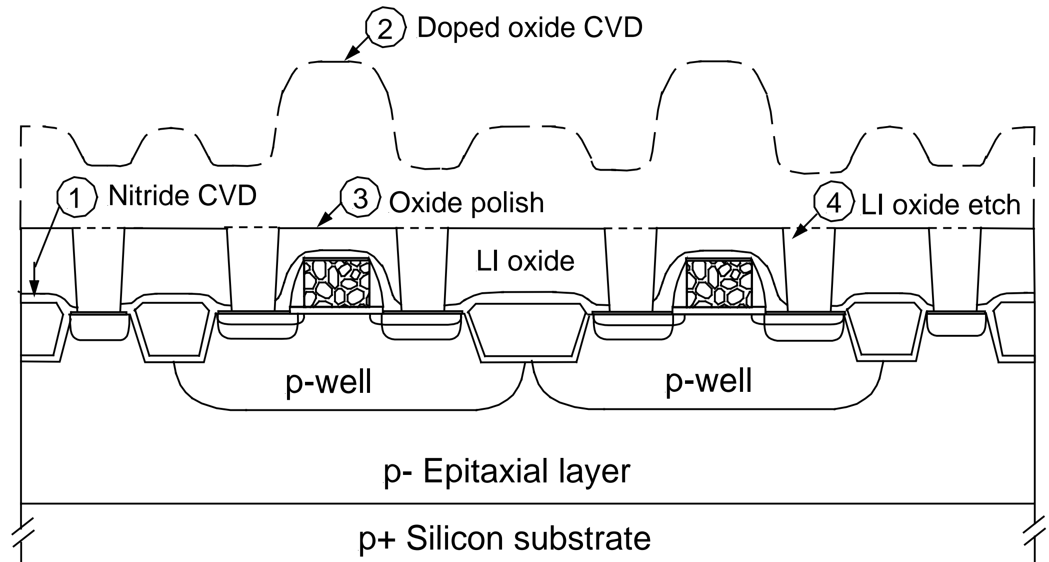
Chemicals etch away the unreacted Ti, leaving behind tisilicide over the active silicon areas.

LI Oxide as a Dielectric for Inlaid LI Metal (Damascene) & LI Oxide Dielectric Formation



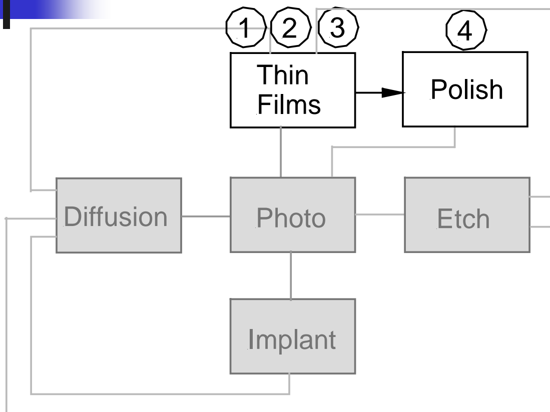
LI : local interconnect

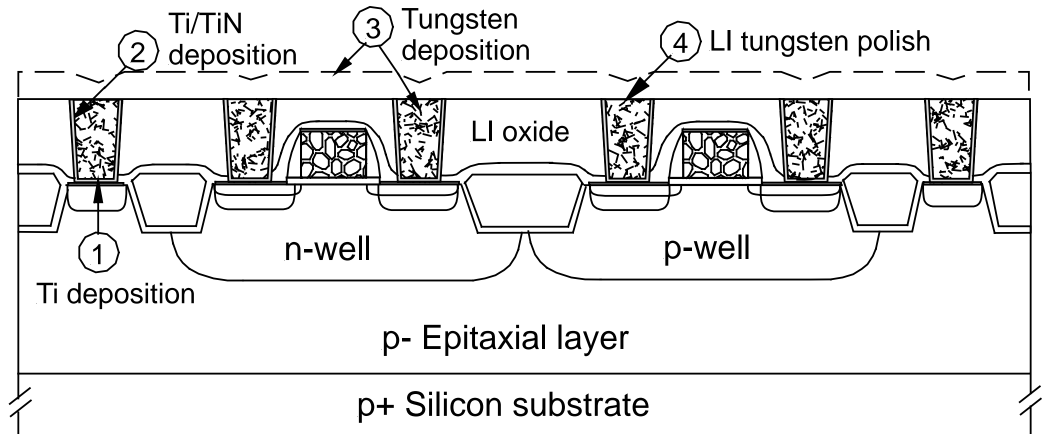




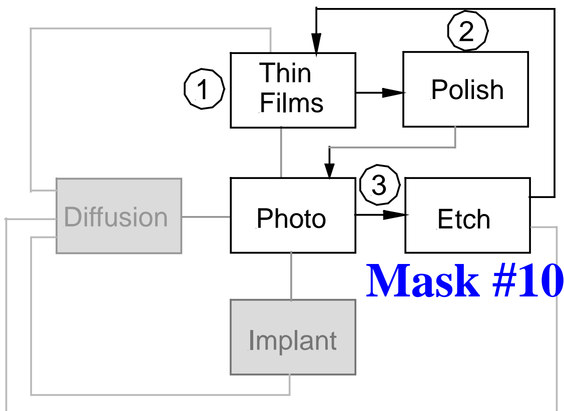
LI Metal Formation & Via-1 Formation

Ti: "double-adhesive tape" to hold W to the SiO2
TiN: a diffusion barrier for the tungsten metal

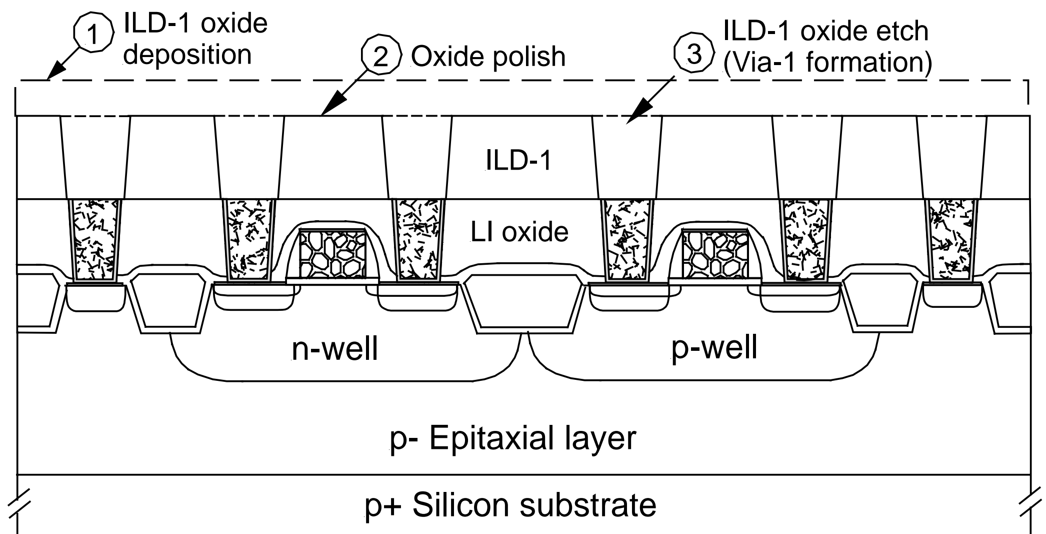




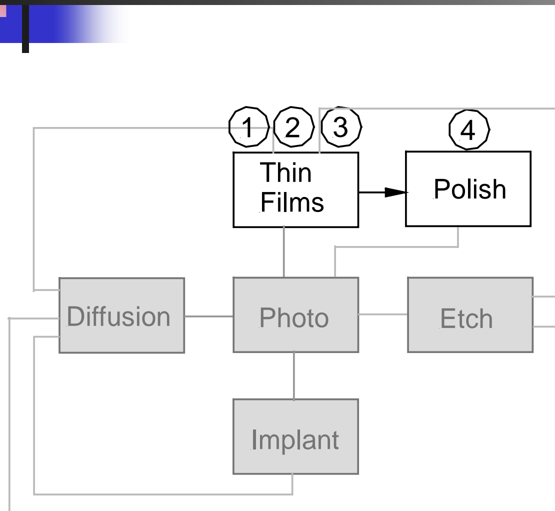
ILD : interlayer dielectric

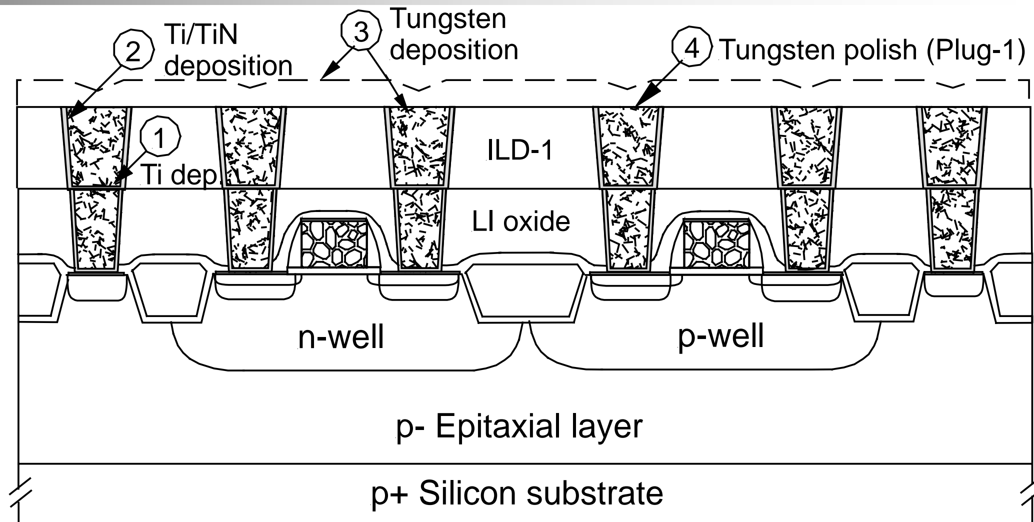


Mask #10



Plug-1 Formation

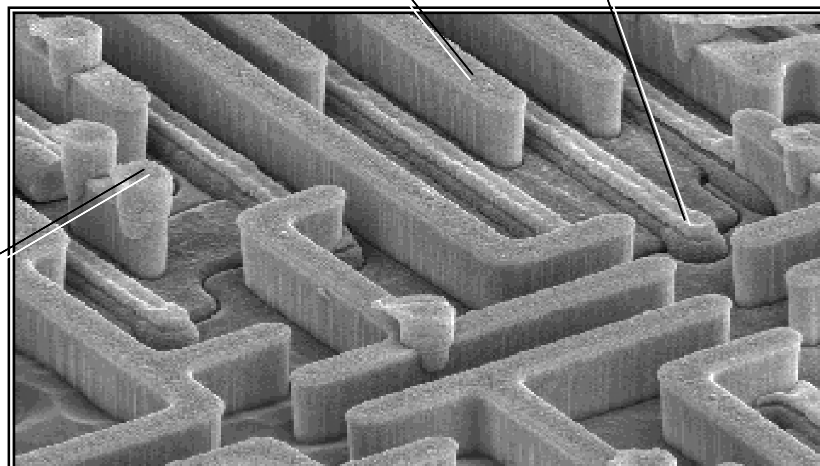




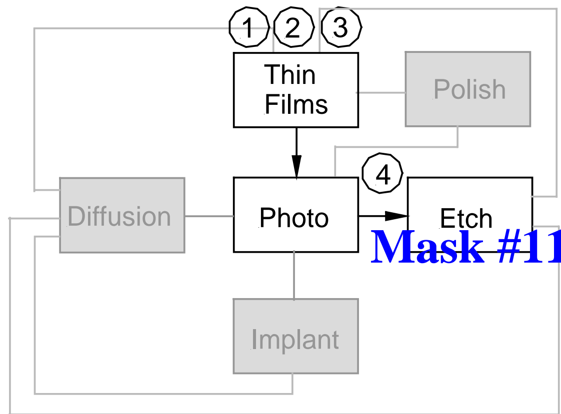
SEM Micrographs of Polysilicon, Tungsten LI and Tungsten Plugs :

Micrograph courtesy of Integrated Circuit Engineering

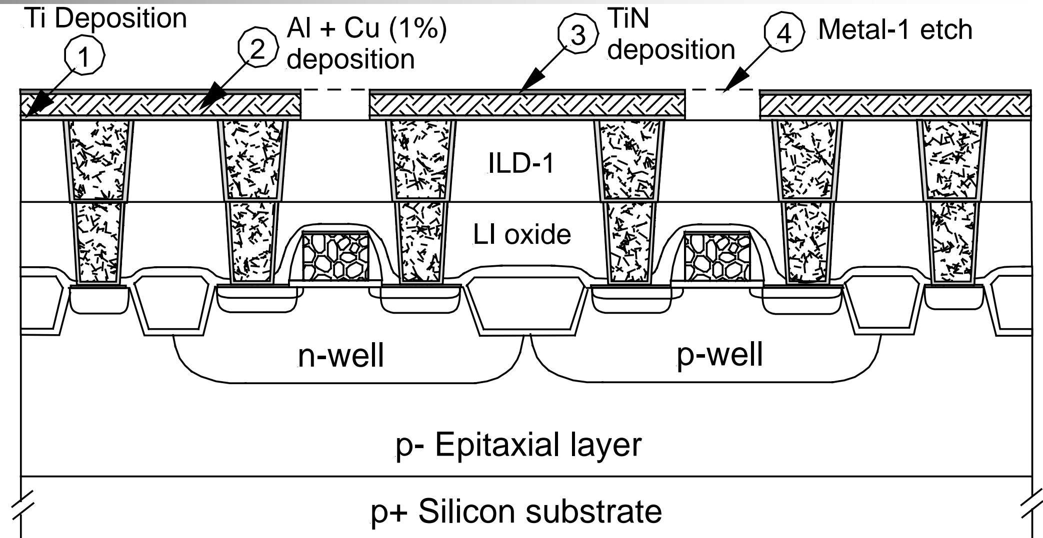
Mag. 17,000 X



Metal-1 Interconnect Formation



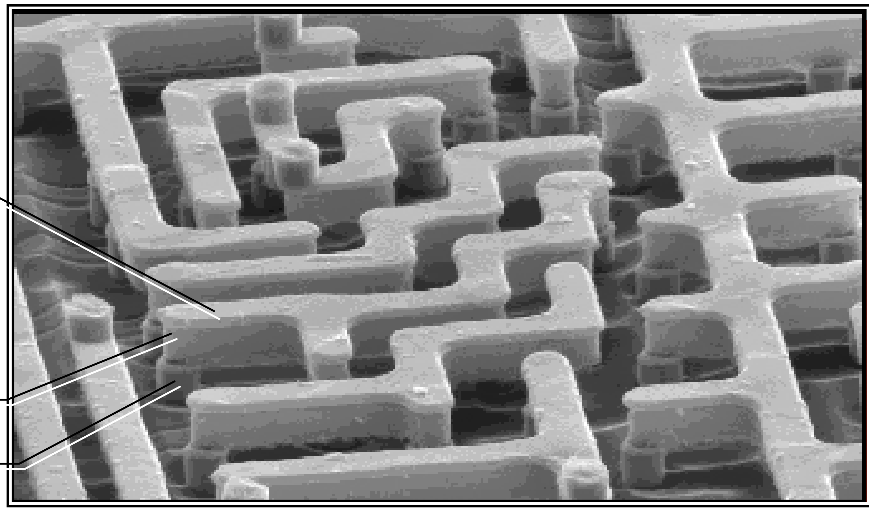
Mask #11



SEM Micrographs of First Metal Layer over First Set of Tungsten Vias :

Micrograph courtesy of Integrated Circuit Engineering

Mag. 17,000 X

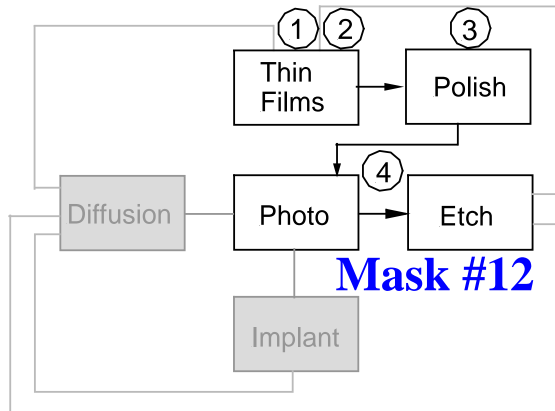


TiN metal cap

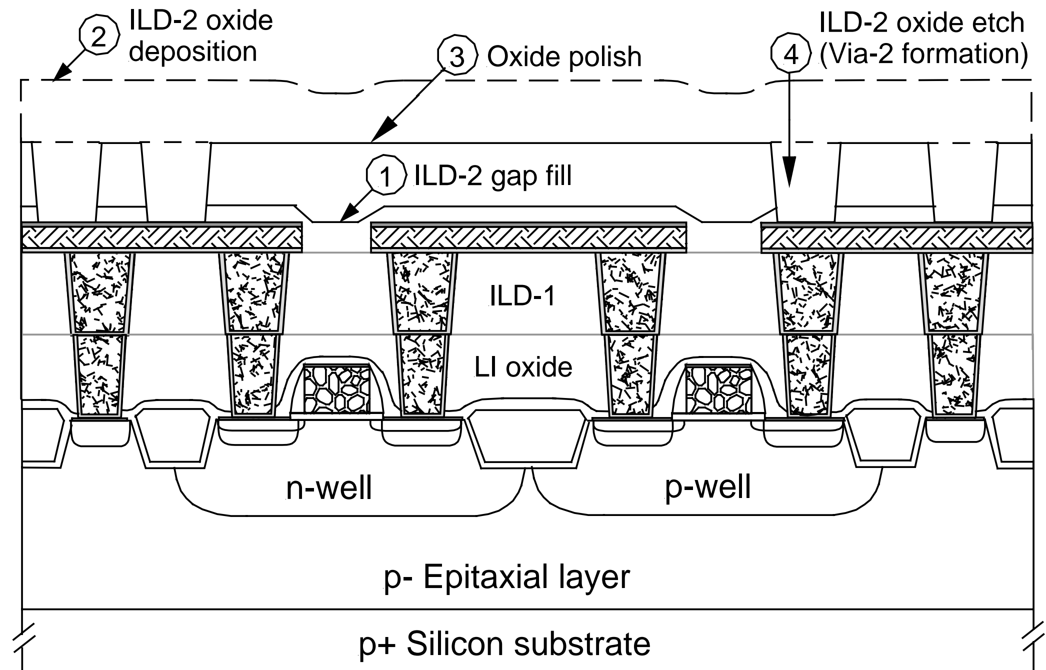
Metal 1, Al

Tungsten plug

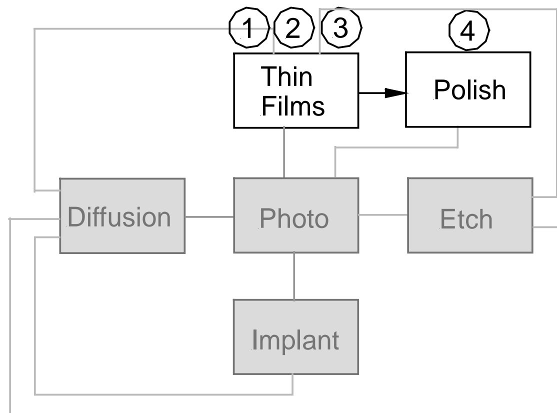
Via-2 Formation

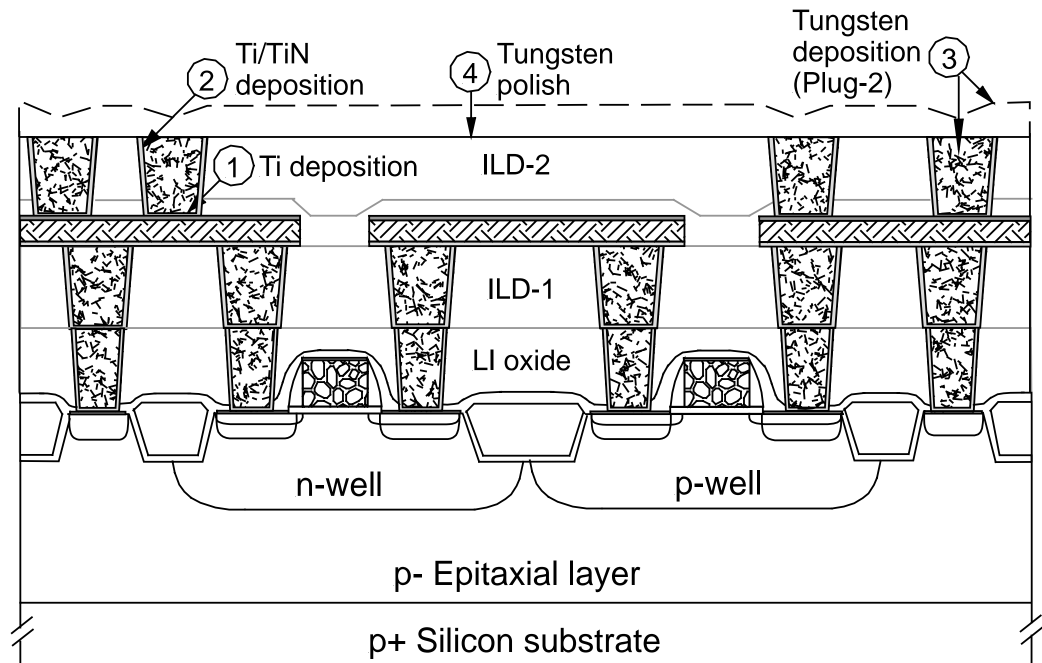


Mask #12

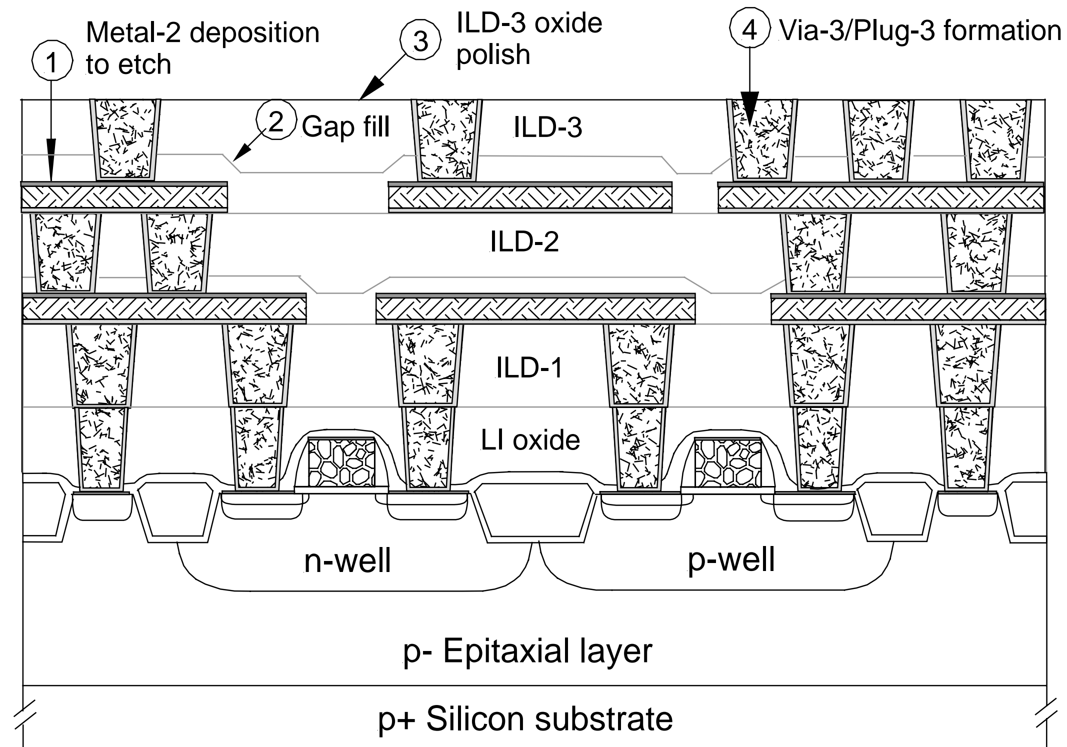


Plug-2 Formation

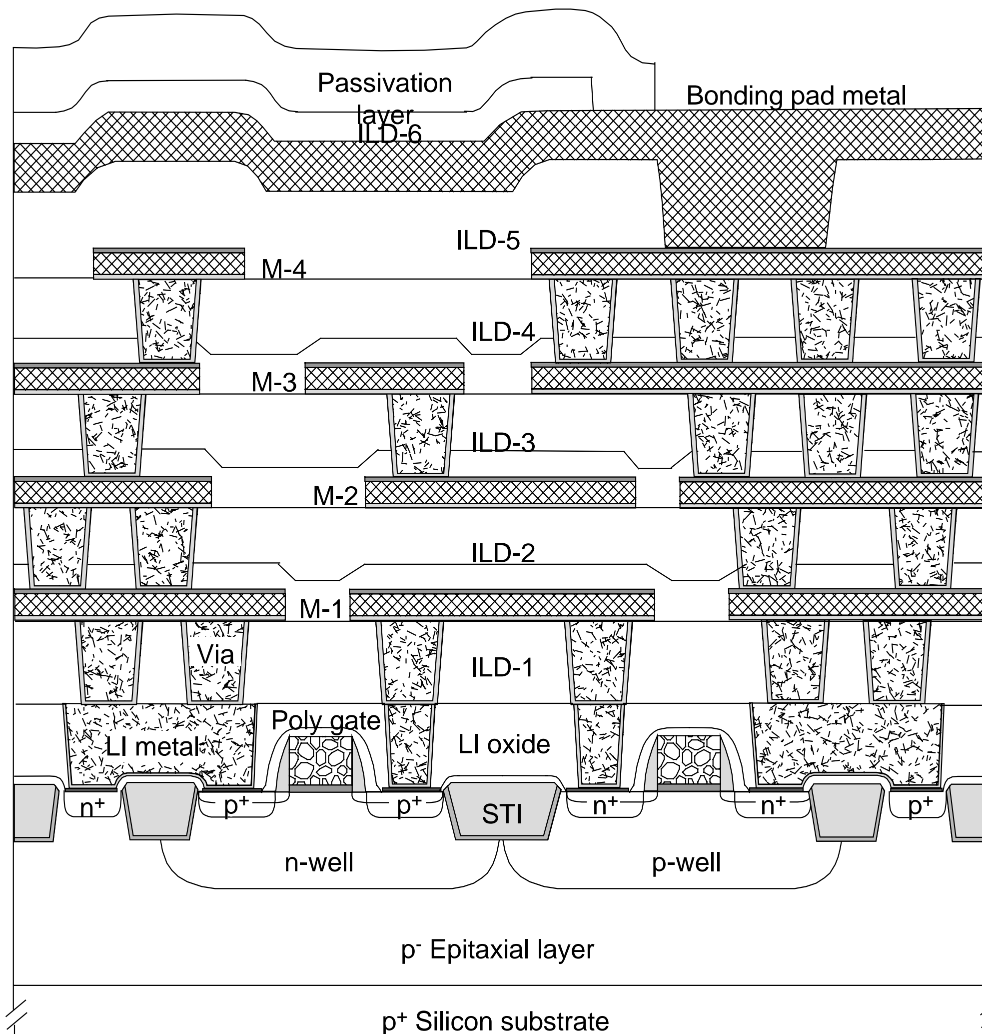




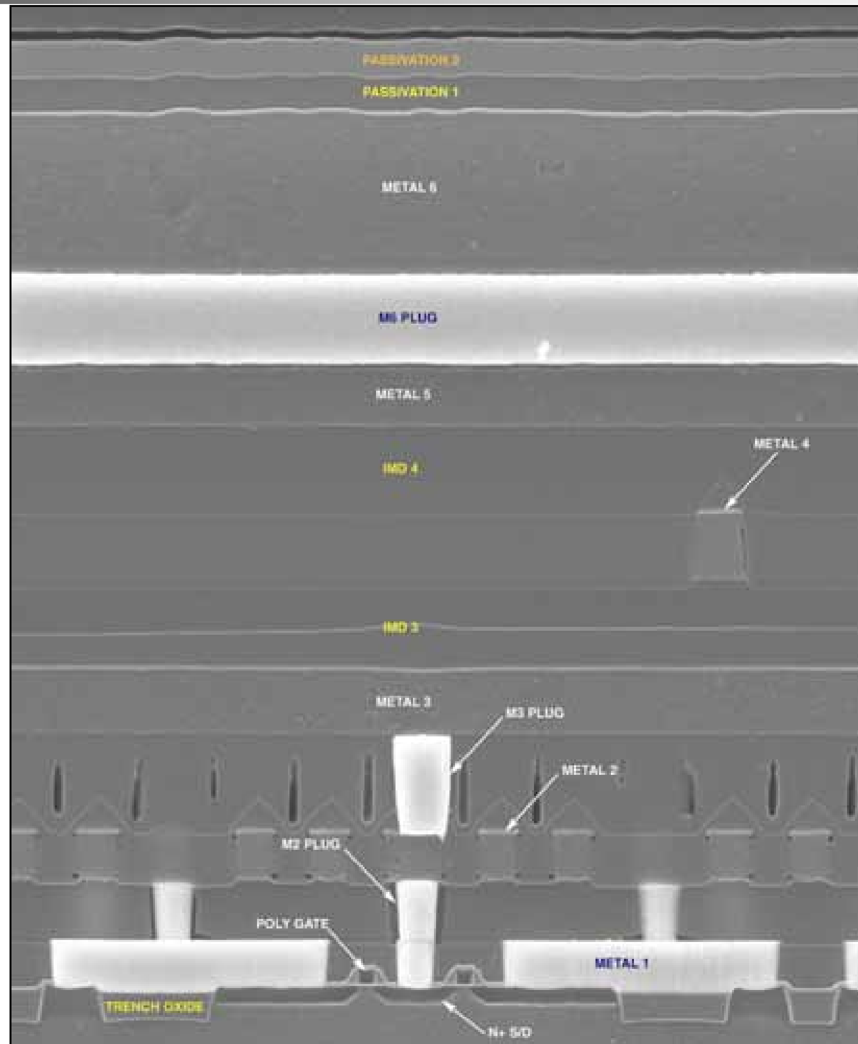
Metal-2 Interconnect Formation



Full 0.18 mm CMOS Cross Section



SEM Micrograph of Cross-section of AMD Microprocessor



Micrograph courtesy of Integrated Circuit Engineering

Mag. 18,250 X

Micromanipulator Prober (Parametric Testing)

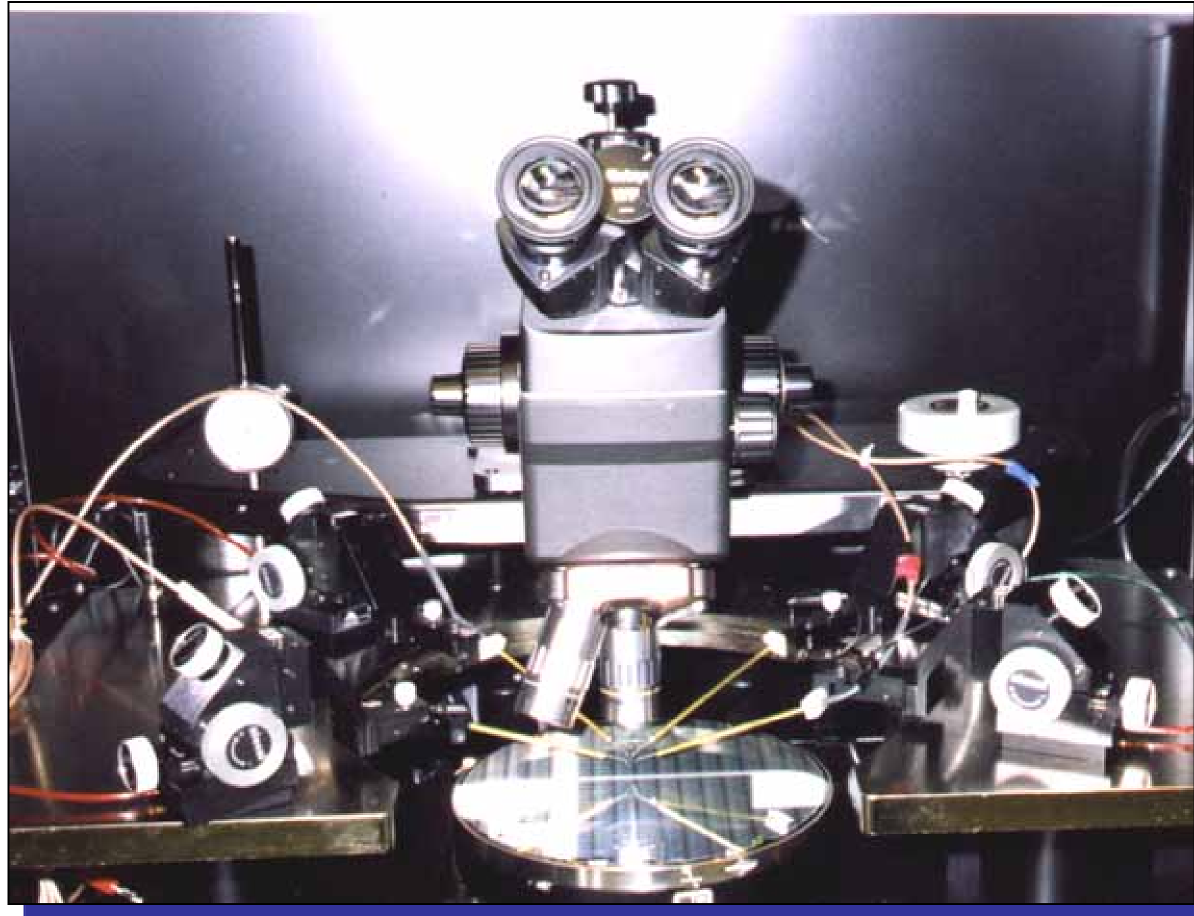


Photo courtesy of Advanced Micro Devices