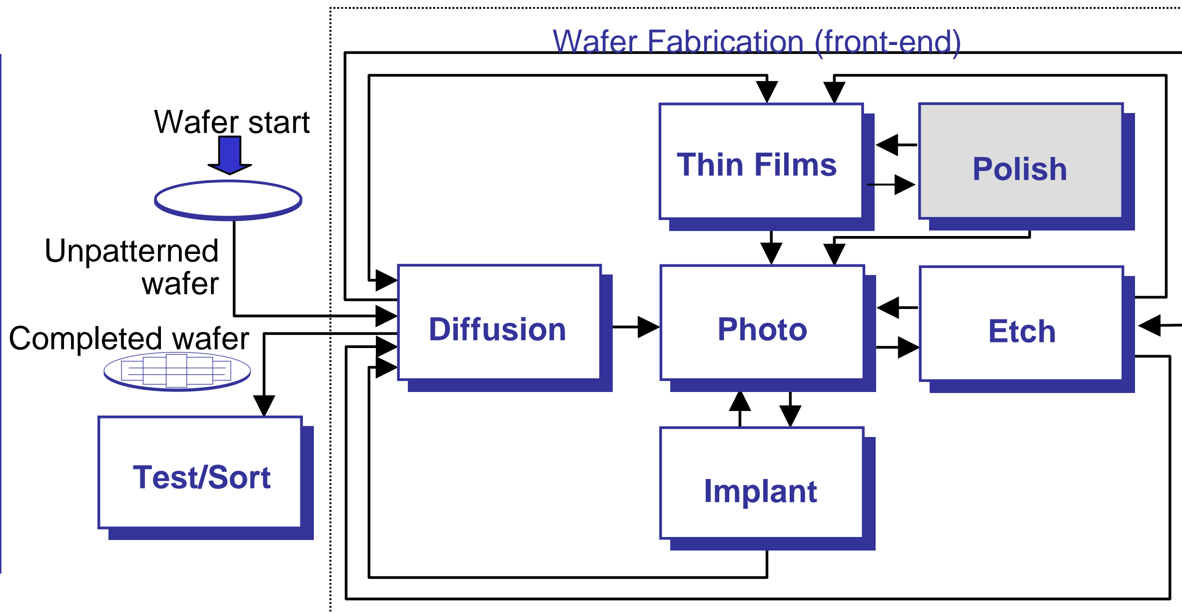
Chapter 3 : ULSI Manufacturing Technology
- (e) Chemical Mechanical Planarization

Reference

1. Semiconductor Manufacturing Technology
   : Michael Quirk and Julian Serda (2001)
2. 國家矽導計畫-教育部晶片法商學程教材 (2004)
3. Semiconductor Physics and Devices- Basic Principles(3/e)
   : Donald A. Neamen (2003)
4. Semiconductor Devices - Physics and Technology (2/e)
   : S. M. Sze (2002)
5. ULSI Technology *: C. Y. Chang, S. M. Sze (1996)*

Polish

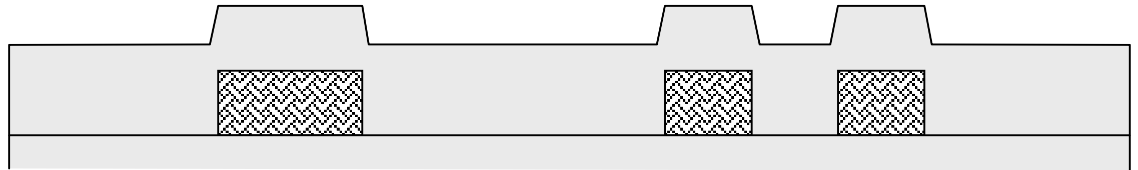
Polish Bay
in a Sub-micron Wafer Fab



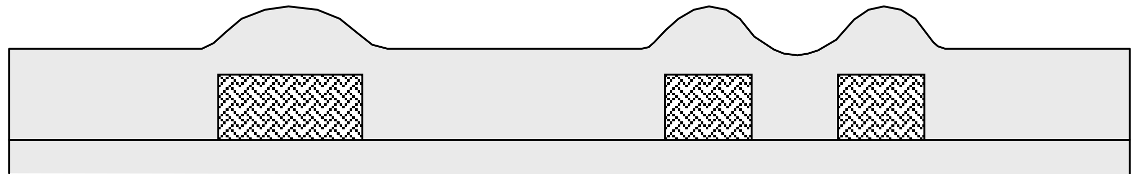
Wafer Process Flow with CMP

Qualitative Definitions of Planarization

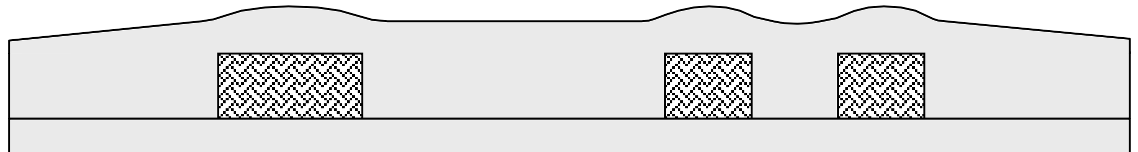
a) No planarization



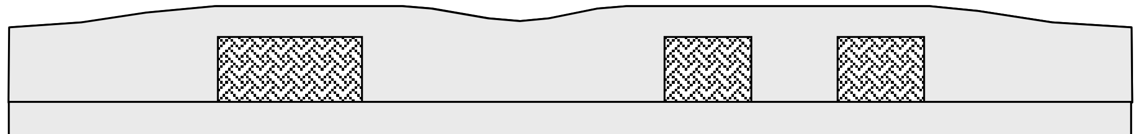
b) Smoothing



c) Partial planarization

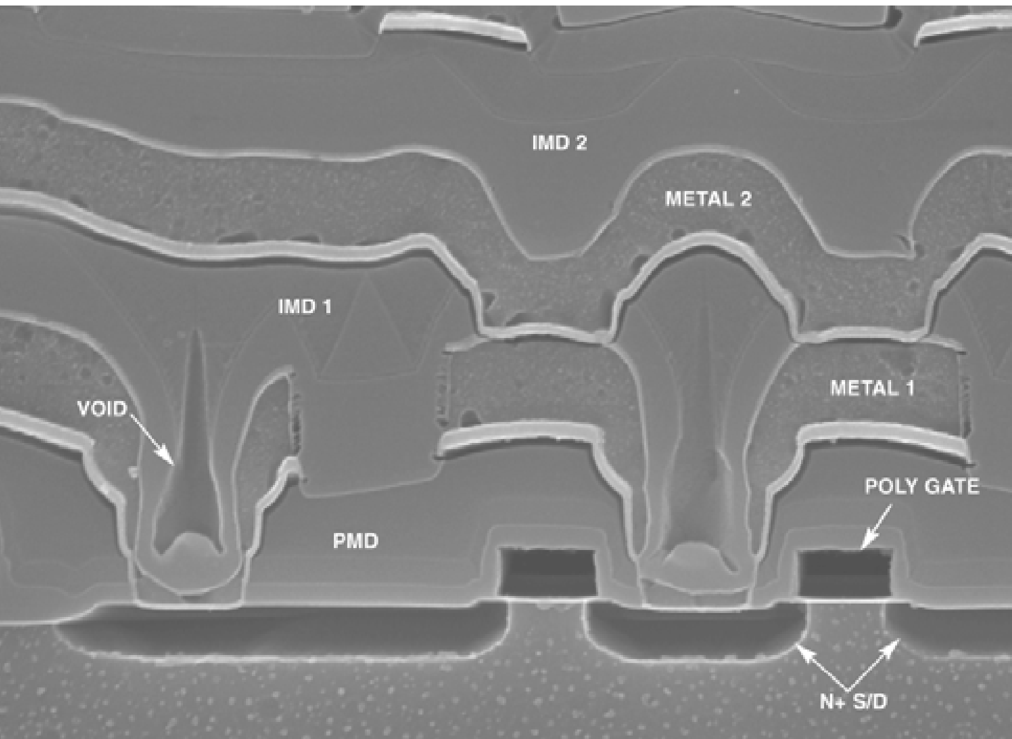


d) Local planarization

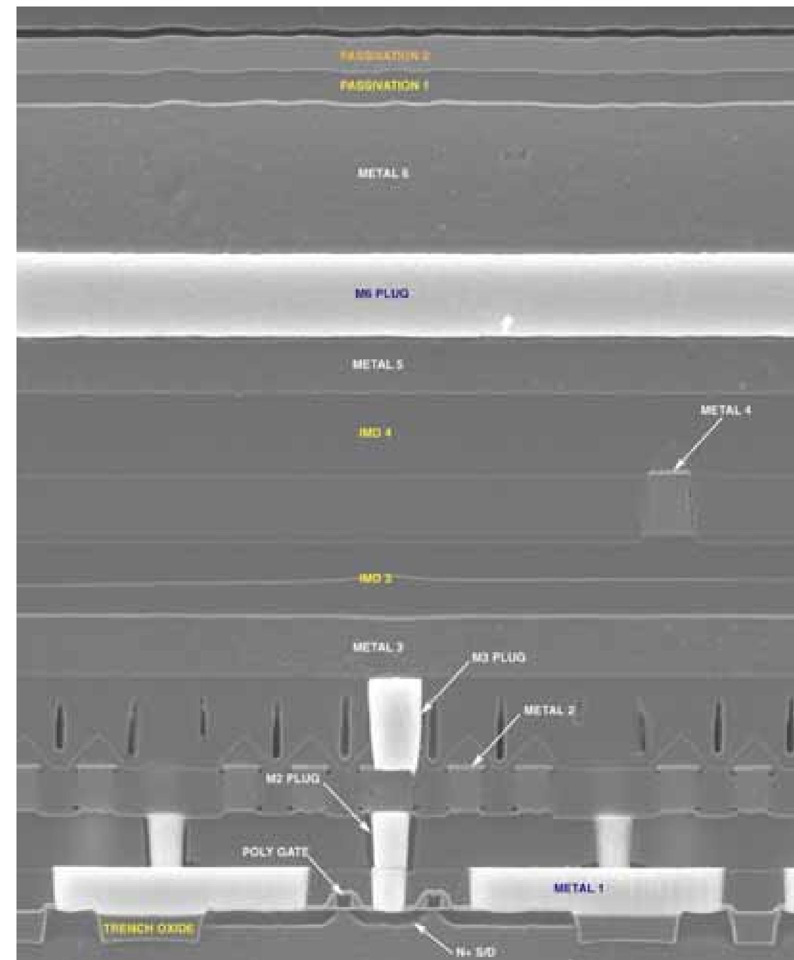


e) Global planarization

Multilayer Metallization with Non-planarized and Planarized Surfaces



Non-planarized IC product



Planarized IC product

Tranditional Planarization

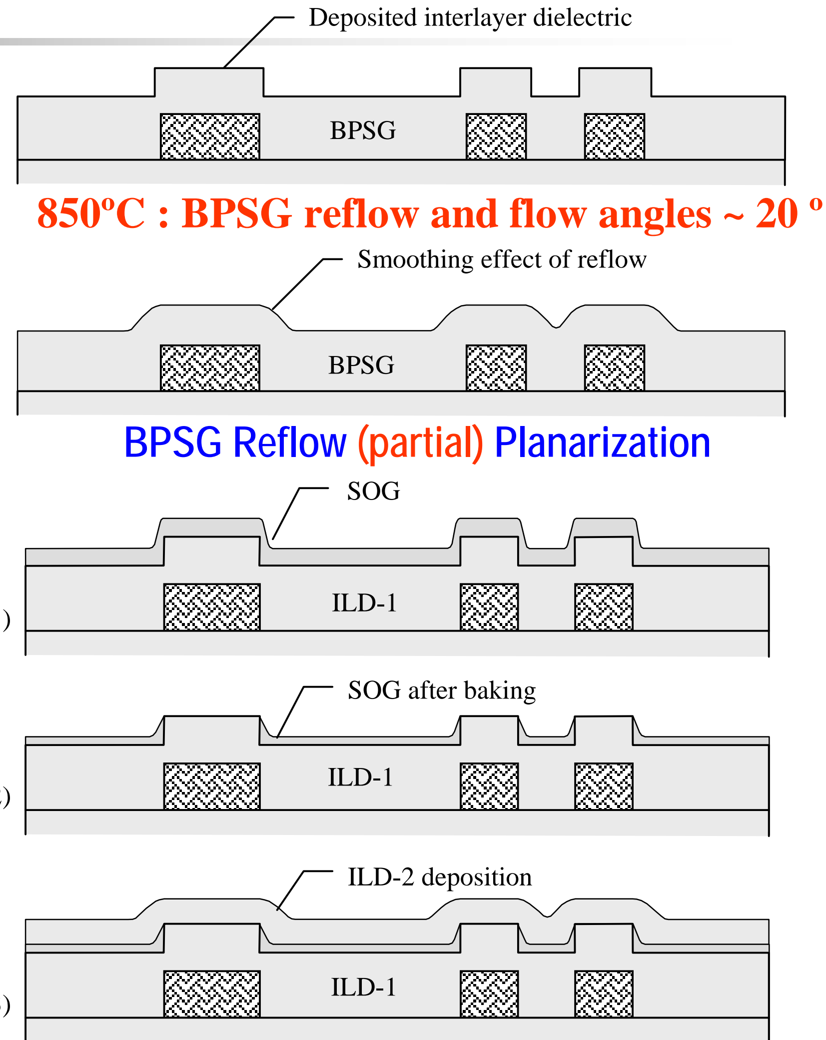
1. Etchback Planarization 2. BPSG Reflow Planarization 3. Spin On film with Etchback

Planarizing material
(Sacrificial layer)
Undesirable topography
Resist or SOG
SiO_2

dry etch

Topography after etchback
SiO_2

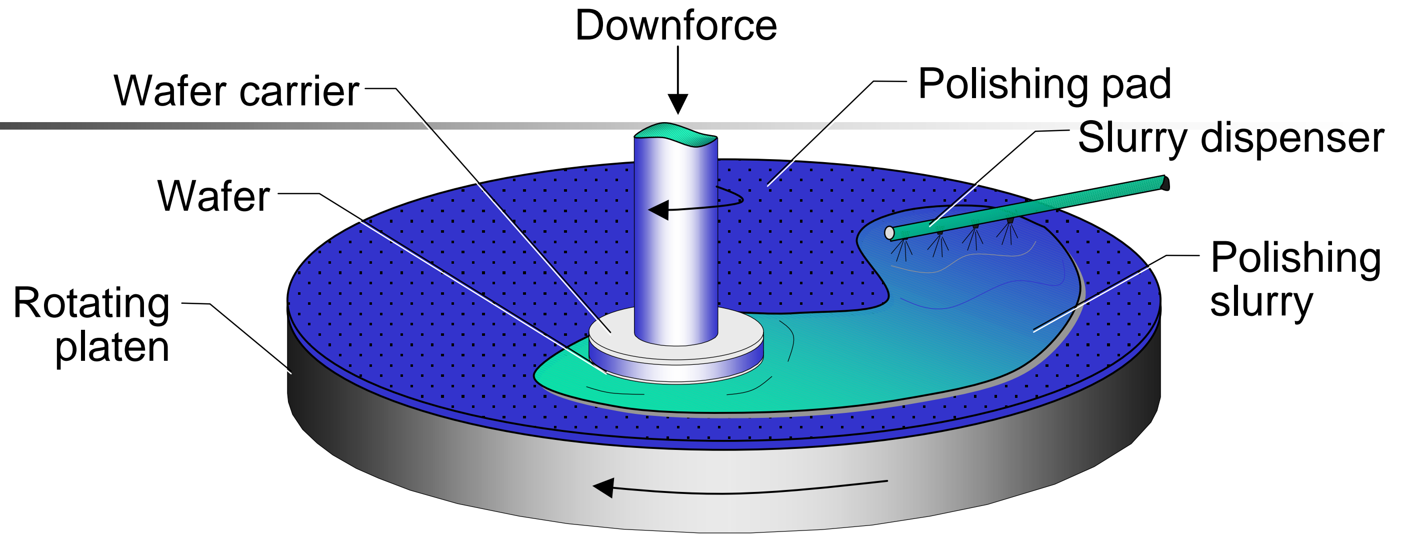
Etchback (local) Planarization



Etching of the sacrificial layer is then done using a dry etch to smooth the surface features by removing high features at a faster rate than low features.

Chemical Mechanical Planarization (CMP)

adequate for deep submicron ICs (global planarization)



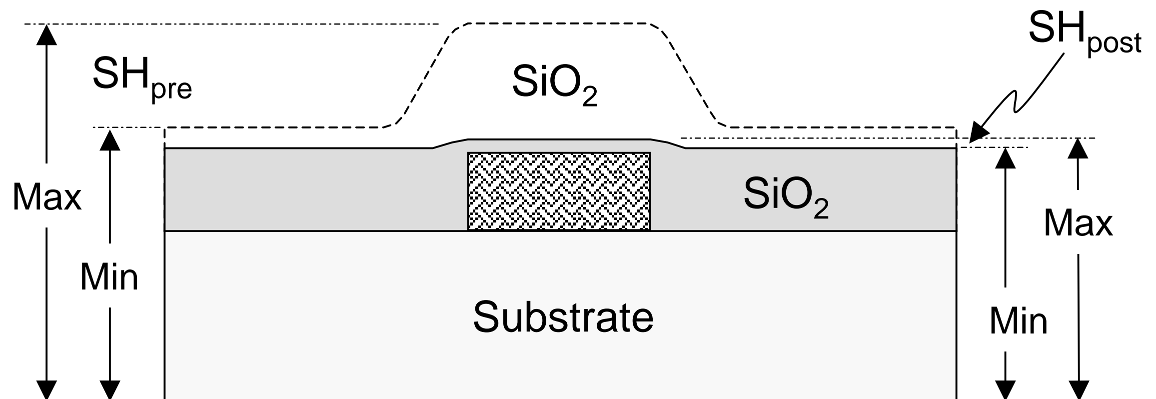
Pre-polish measurement

Post-polish measurement

Degree of planarization:

$$DP(\%) = (1 - \frac{SH_{post}}{SH_{pre}}) \times 100$$

SH: Distance between the maximum and minimum step heights



Wafer Measurements for Degree of Planarization

Advantages of CMP

Benefits	Remarks
1. Planarization	Achieves global planarization.
2. Planarize different materials	Wide range of wafer surfaces can be planarized.
3. Planarize multi-material surfaces	Useful for planarizing multiple materials during the same polish step.
4. Reduce severe topography	Reduces topography to allow for fabrication with tighter design rules and additional interconnection levels.
5. Alternative method of metal patterning	Provides an alternate means of patterning metal (e.g., Damascene process), eliminating the need of the plasma etching for difficult-to-etch metals and alloys.
6. Improved metal step coverage	Improves metal step coverage due to reduction in topography.
7. Increased IC reliability	Contributes to increasing IC reliability, speed and yield (lower defect density) of sub-0.5μm devices and circuits.
8. Reduce defects	CMP is a subtractive process and can remove surface defects.
9. No hazardous gases	Does not use hazardous gases common in dry etch process.

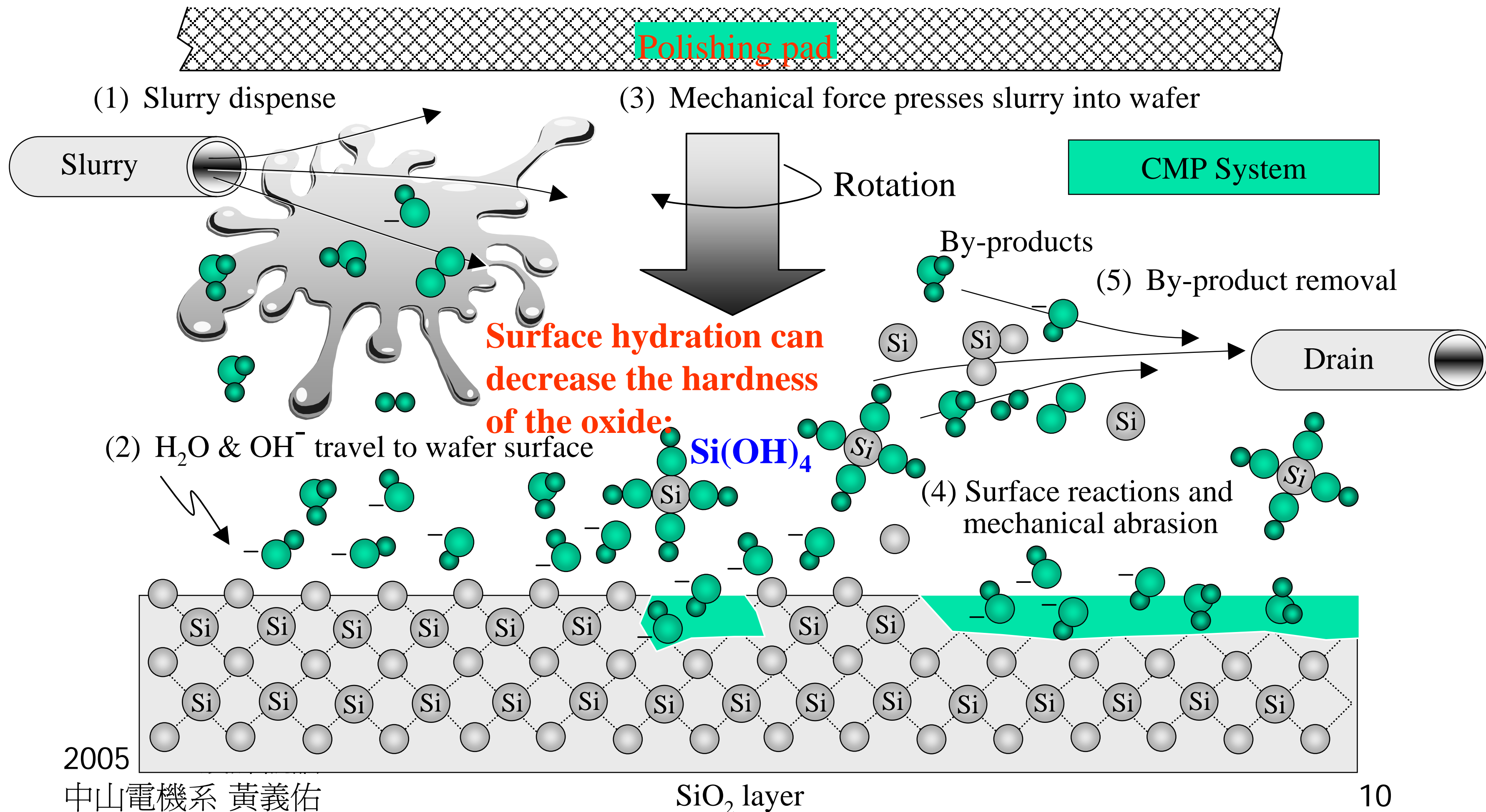
Disadvantages of CMP

Disadvantages	Remarks
1. New technology	CMP is a new technology for wafer planarization. There is relatively poor control over the process variables with a narrow process latitude.
2. New defects	New types of defects from CMP can affect die yield. These defects become more critical for sub-0.25 μm feature sizes.
3. Need for additional process development	CMP requires additional process development for process control and metrology. An example is the endpoint of CMP is difficult to control for a desired thickness.
4. Cost of ownership is high	CMP is expensive to operate because of costly equipment and consumables. CMP process materials require high maintenance and frequent replacement of chemicals and parts.

CMP Mechanism : Oxide Polish

(1) A chemical reaction by the slurry chemistry forms a wafer surface layer that is relatively easy to remove

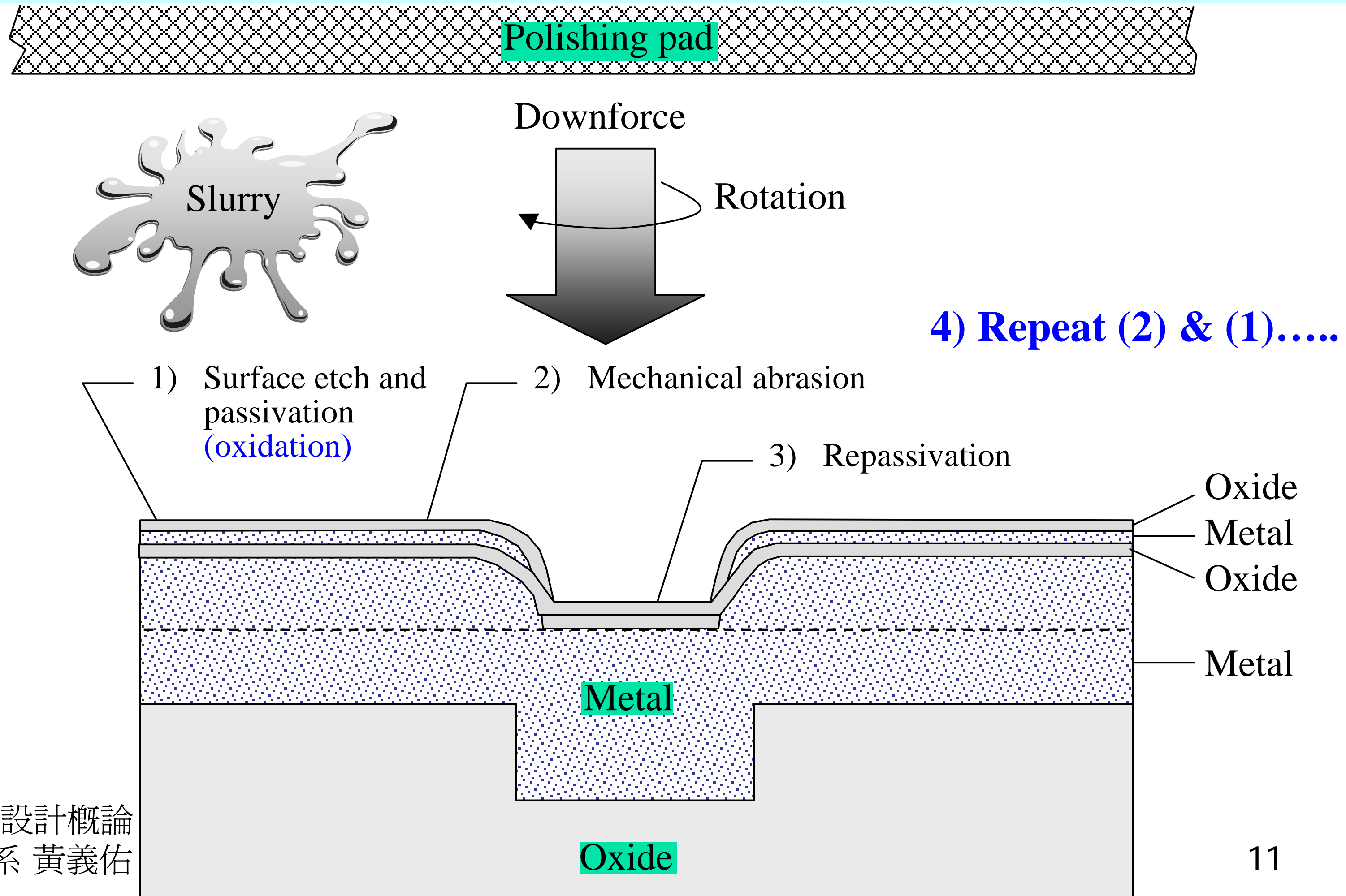
(2) This reacted surface layer is mechanically removed by the slurry abrasive component and the applied pressure and relative velocity of a polishing pad.



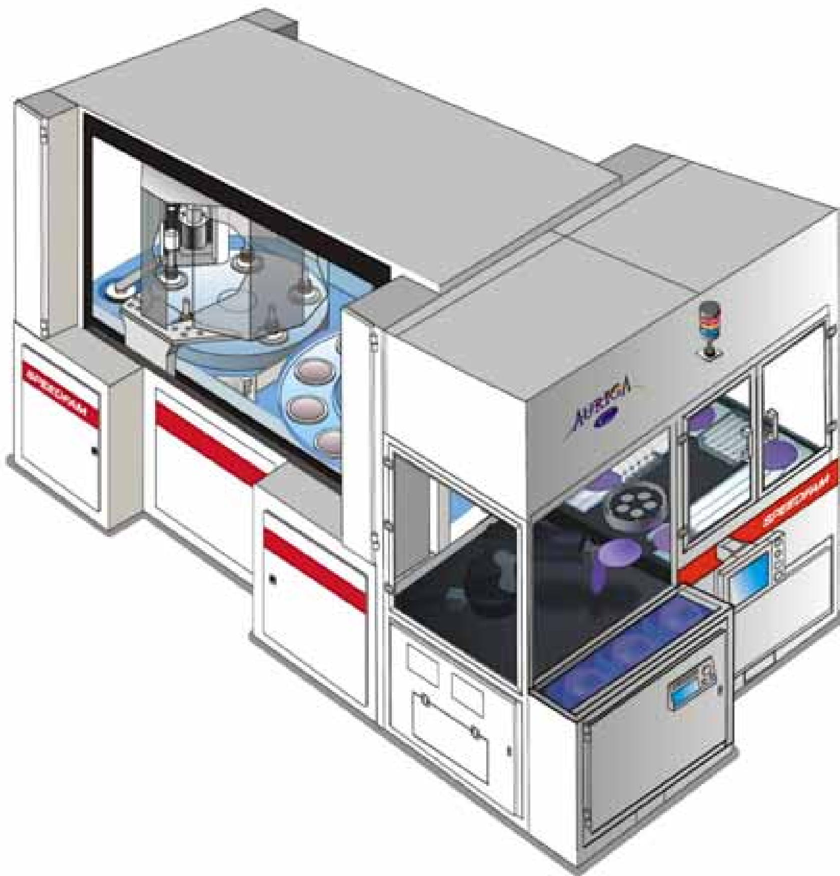
Mechanism for Metal CMP

(1) **Chemical oxidation mechanism:** the slurry comes in contact with the metal surface and oxidizes it.

(2) **Mechanical abrasion mechanism:** the metal oxide layer is then removed by mechanical abrasion from the particles in the slurry.



CMP Tool



CMP Polishing Pad