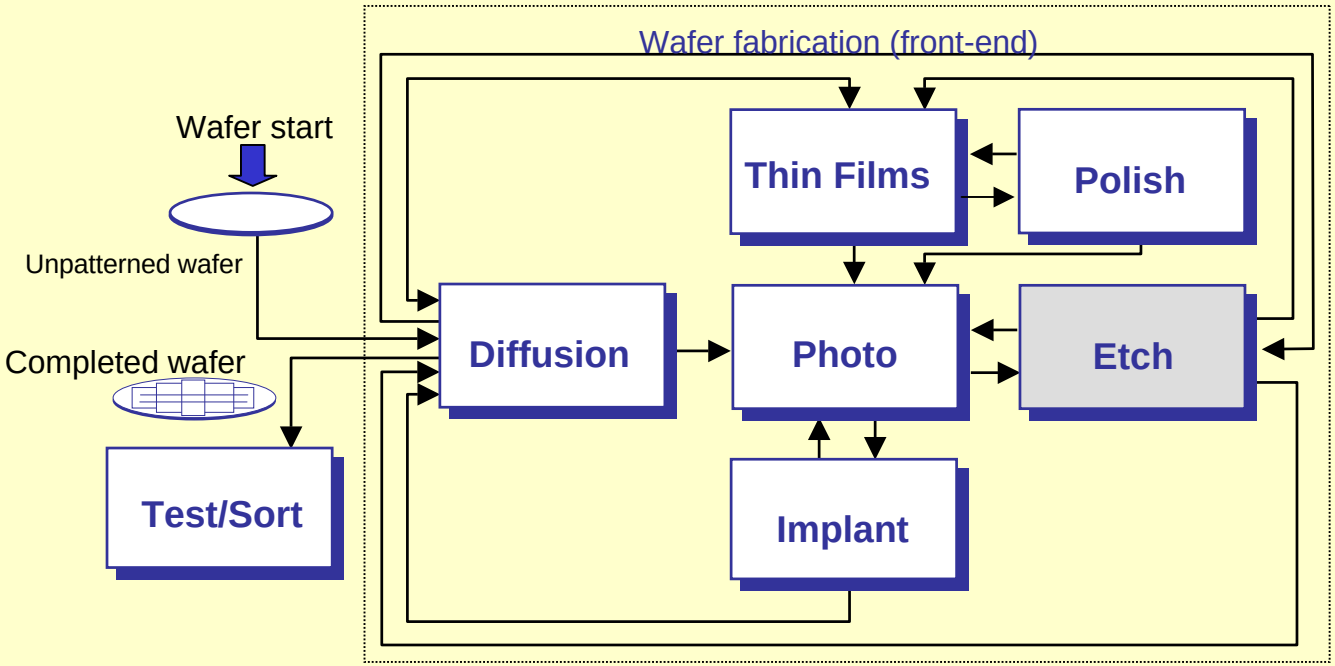
Chapter 3 : ULSI Manufacturing Technology – (d) Etch

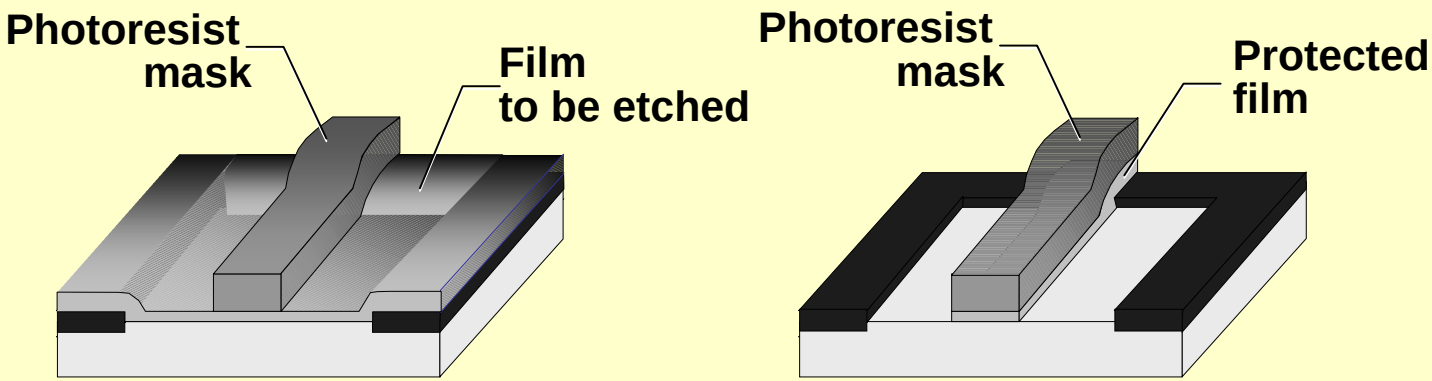
Reference

1. **Semiconductor Manufacturing Technology**
   : Michael Quirk and Julian Serda (2001)
2. **國家矽導計畫-教育部晶片法商學程教材 (2004)**
3. **Semiconductor Physics and Devices- Basic Principles(3/e)**
   : Donald A. Neamen (2003)
4. **Semiconductor Devices - Physics and Technology (2/e)**
   : S. M. Sze (2002)
5. **ULSI Technology *: C. Y. Chang, S. M. Sze (1996)***

Applications for Wafer Etch in CMOS Technology

Process Flow in a Wafer Fab :





(a) Photoresist-patterned substrate (b) Substrate after etch

Etch Process & Etch Parameters

Categories of Etch Processes:

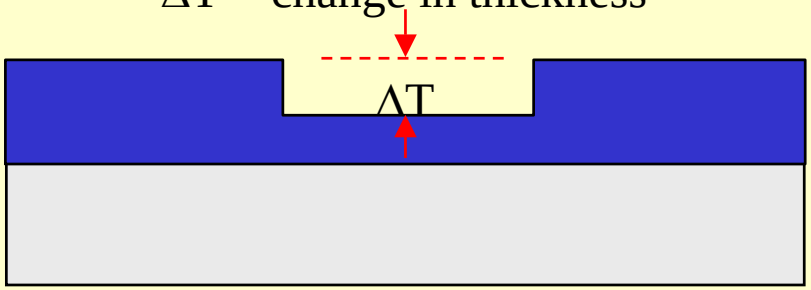
- Wet Etch
- Dry Etch
- Three Major Materials to be Etched:
  - Silicon
  - Dielectric
  - Metal
- Patterned Etch Versus Unpatterned Etch

- Etch rate
- Etch profile
- Etch bias
- Selectivity
- Uniformity
- Residues
- Polymer formation
- Plasma-induced damage
- Particle contamination and defects

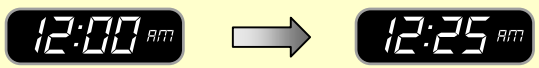
Isotropic & Anisotropic Etch

Etch Rate & Wet Chemical Isotropic Etch

ΔT = change in thickness

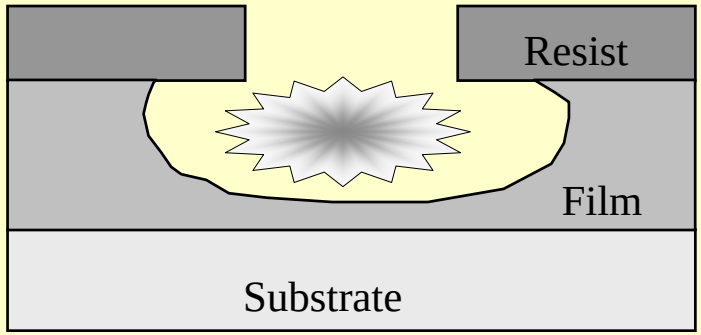


t = elapsed time during etch



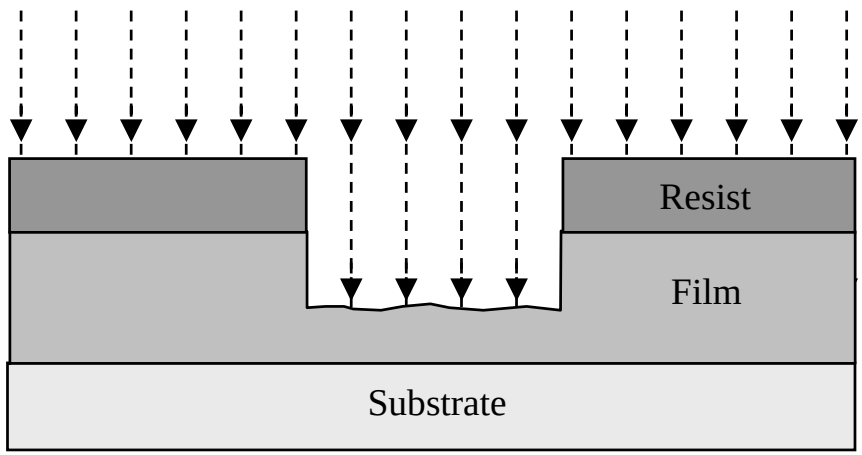
Start of etch End of etch

Isotropic etch - etches in all directions at the same rate



Anisotropic Etch with Vertical Etch Profile

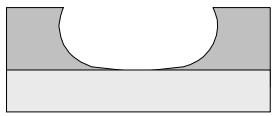
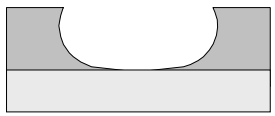
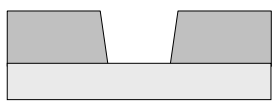
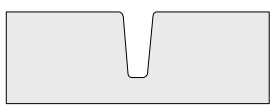
Anisotropic etch - etches in only one direction



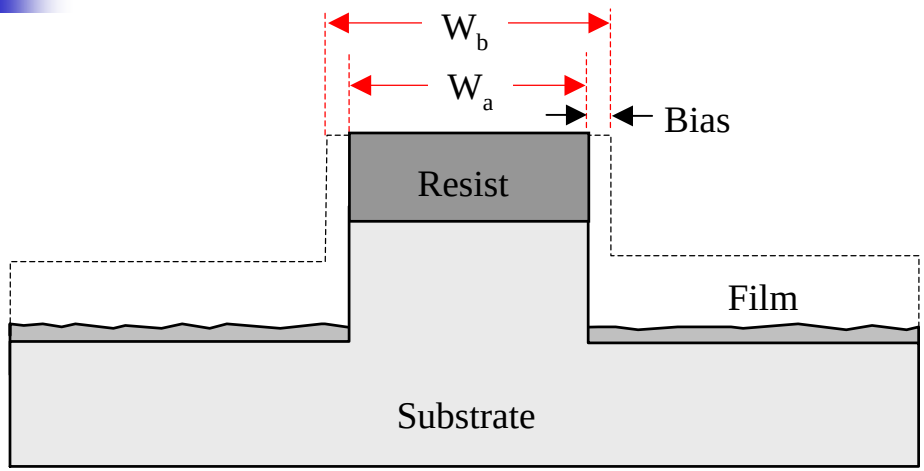
Advantages of Dry Etch over Wet Etch

1. Etch profile is anisotropic with excellent control of sidewall profiles.
2. Good CD control.
3. Minimal resist lifting or adhesion problems.
4. Good etch uniformity within wafer, wafer-to-wafer and lot-to-lot.
5. Lower chemical costs for usage and disposal.

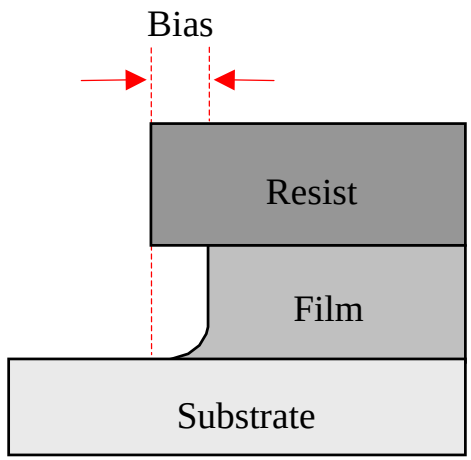
Sidewall Profiles for Wet Etch Versus Dry Etch

Type of Etch	Sidewall Profile	Diagram
Wet Etch	Isotropic	
Dry Etch	Isotropic (depending on equipment & parameters)	
	Anisotropic (depending on equipment & parameters)	
	Anisotropic – Taper	
	Silicon Trench	

Etch Bias & Etching Undercut



(a)

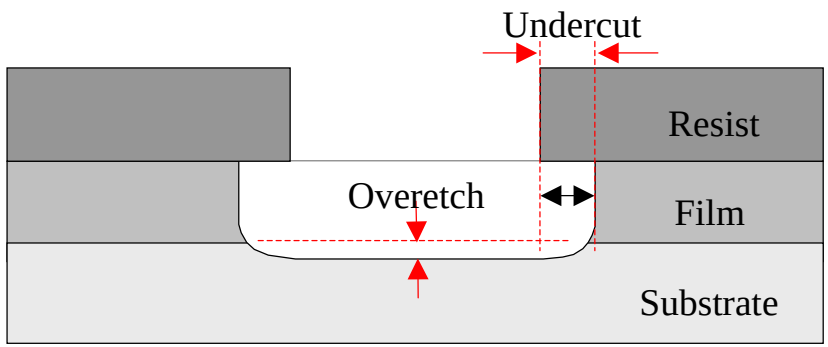


(b)

Etch bias = W_b-W_a

W_b = the original linewidth on photoresist before etch.

W_a = the final linewidth of the etched material after resist removal.

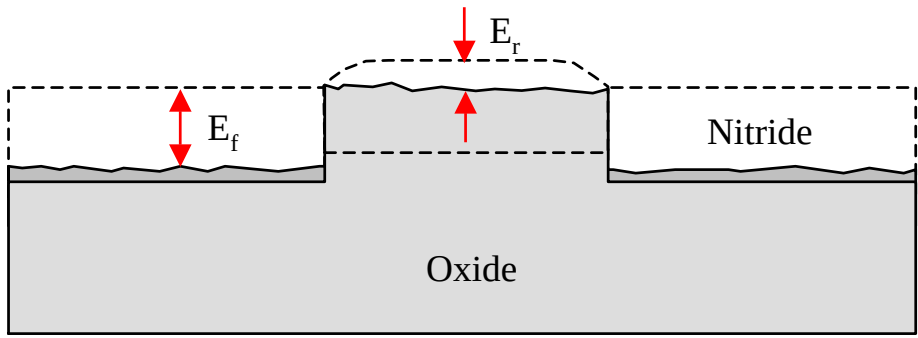


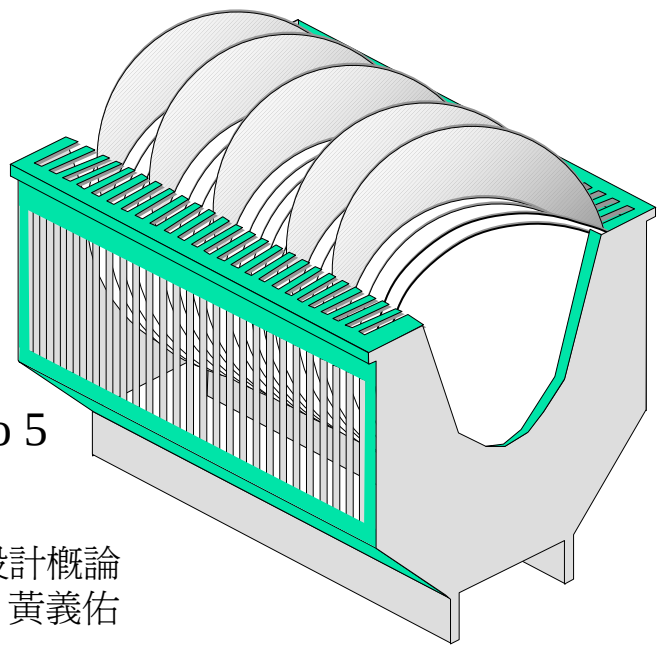
Etch Selectivity & Etch Uniformity

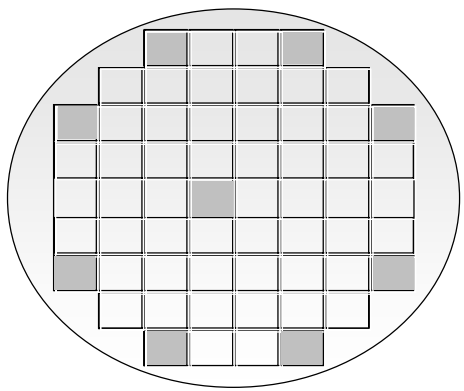
Etch selectivity: $S_R = \frac{E_f}{E_r}$

E_f = the etch rate of the film undergoing etch

E_r = the etch rate of the masking layer (e.g. photoresist)







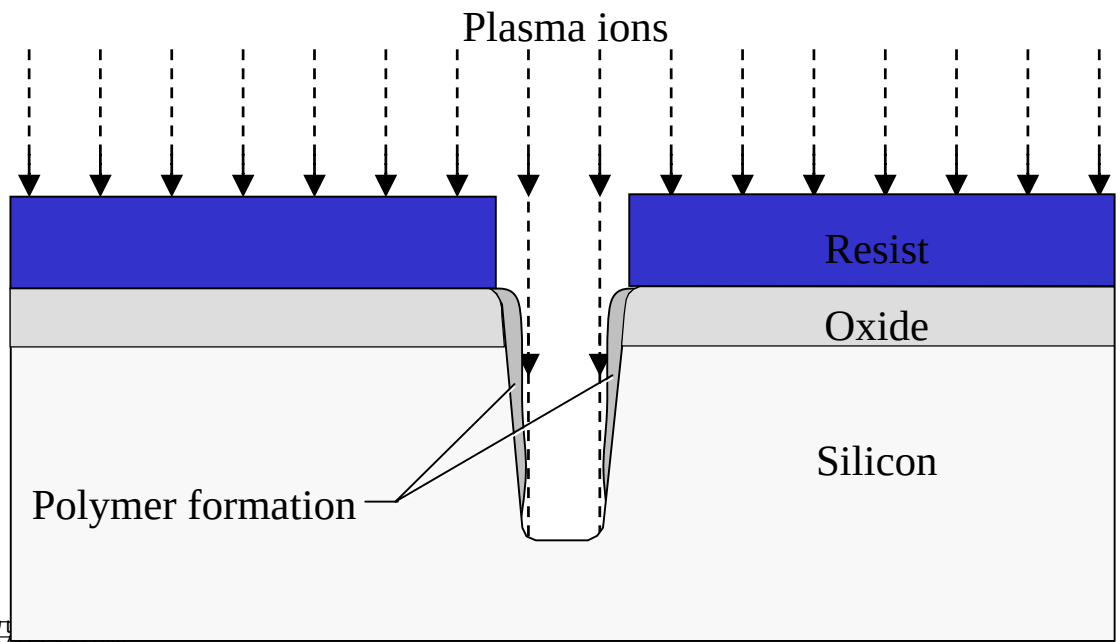
Randomly select 3 to 5 wafers in a lot

Measure etch rate at 5 to 9 locations on each wafer, then calculate etch uniformity for each wafer and compare wafer-to-wafer.

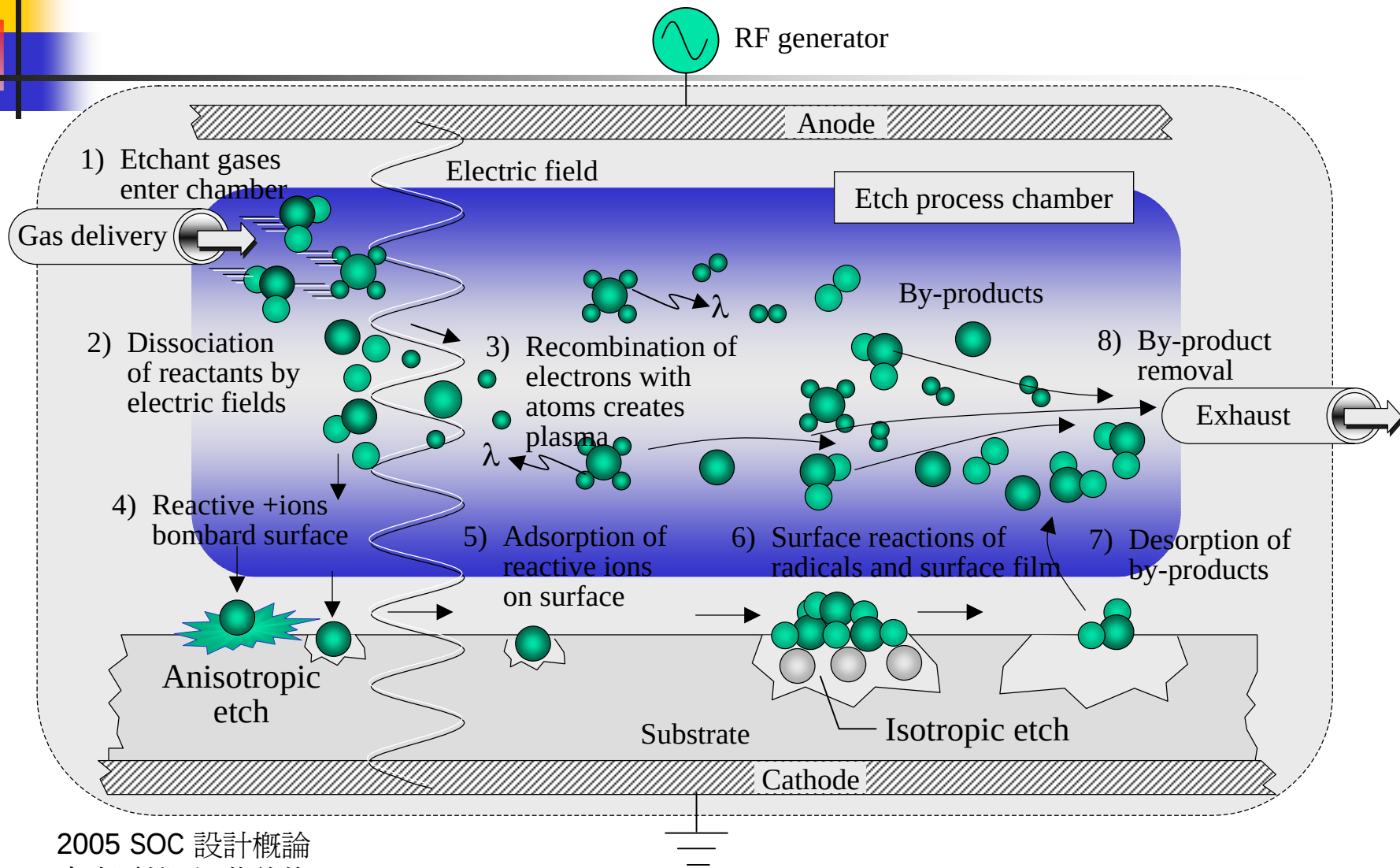
Polymer Sidewall Passivation for Increased Anisotropy

The result is better control of CD of patterened structures. The polymers come from PR carbon converted into polymers during etching and combines with etching gases (i.e. C_2F_4) and etch by-products to form this sidewall polymer.

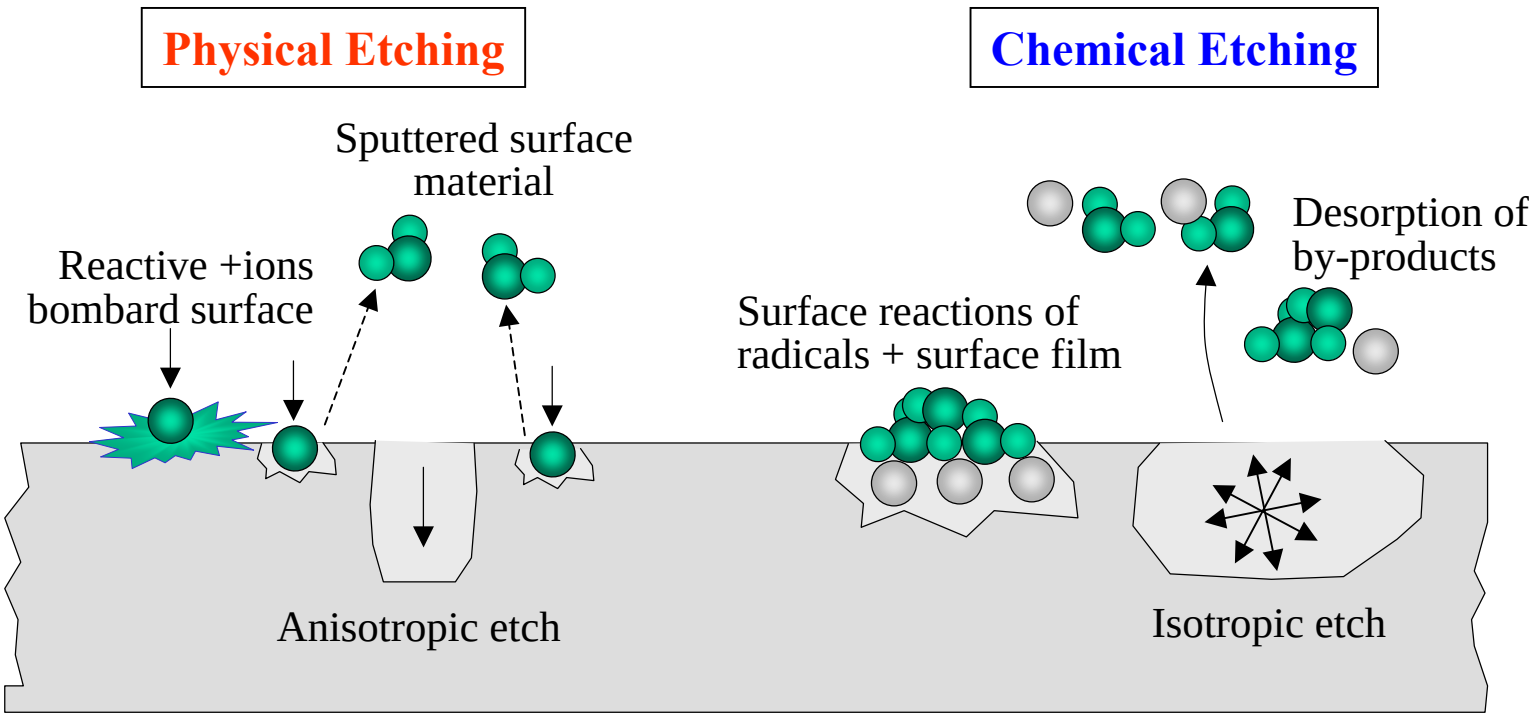
The polymer chains have strong C-F bonds that are difficult to oxidize and remove. However, the polymers must be removed after the etch process or device yield and reliability is affected. The cleaning of the sidewall often requires special gas chemistry for a plasma stripping process or possible a wet clean using strong solvents followed by DI water rinsing.



Plasma Etch Process of a Silicon Wafer



Chemical and Physical Dry Etch Mechanisms



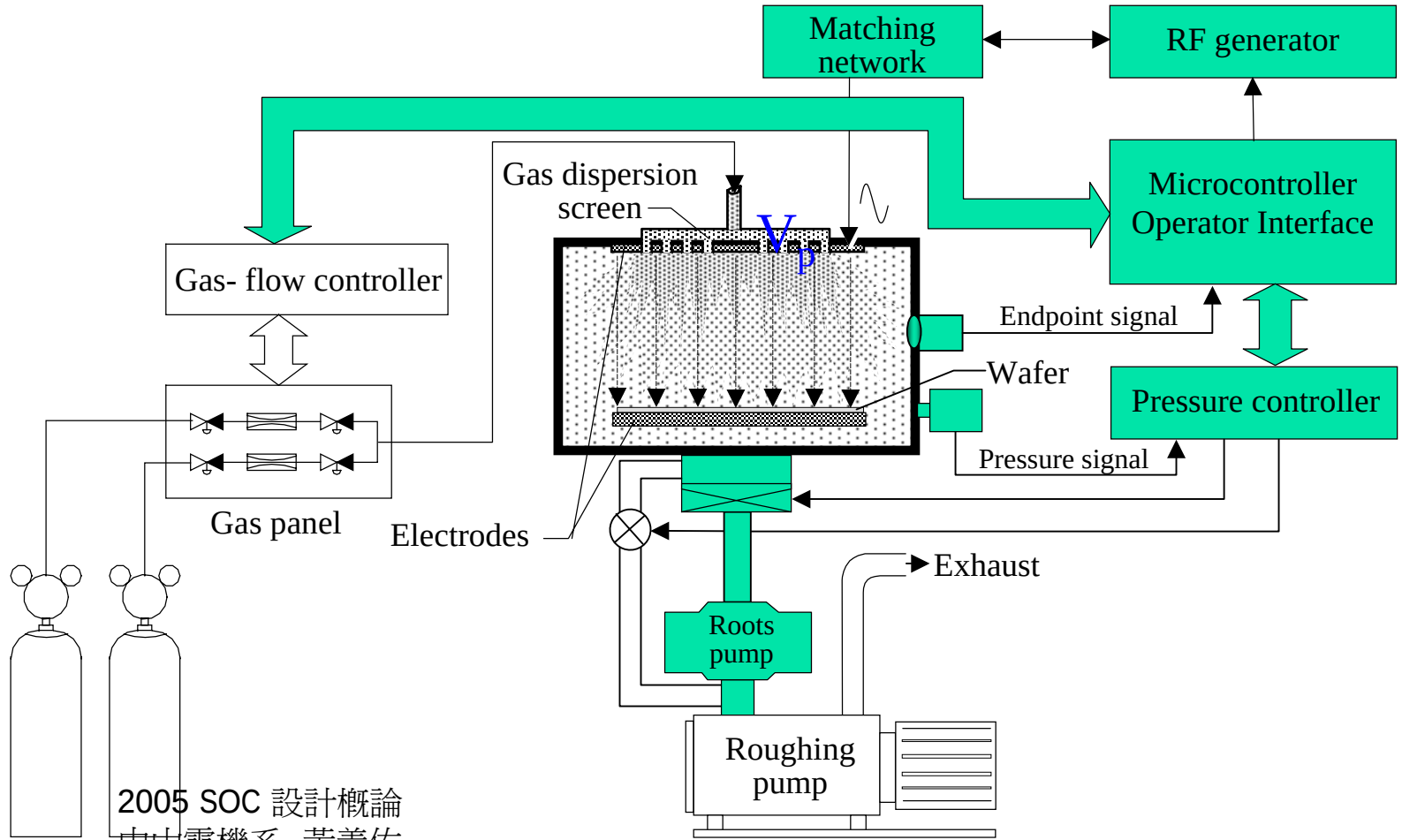
Chemical Versus Physical Dry Plasma Etching

Etch Parameter	Physical Etch (RF field perpendicular to wafer surface)	Physical Etch (RF field parallel to wafer surface)	Chemical Etch	Combined Physical and Chemical
Etch Mechanism	Physical ion sputtering	Radicals in plasma reacting with wafer surface*	Radicals in liquid reacting with wafer surface	In dry etch, etching includes ion sputtering and radicals reacting with wafer surface
Sidewall Profile	Anisotropic	Isotropic	Isotropic	Isotropic to Anisotropic
Selectivity	Poor/difficult to increase (1:1)	Fair/good (5:1 to 100:1)	Good/excellent (up to 500:1)	Fair/good (5:1 to 100:1)
Etch Rate	High	Moderate	Low	Moderate
CD Control	Fair/good	Poor	Poor to non-existent	Good/excellent

* Used primarily for stripping and etchback operations.

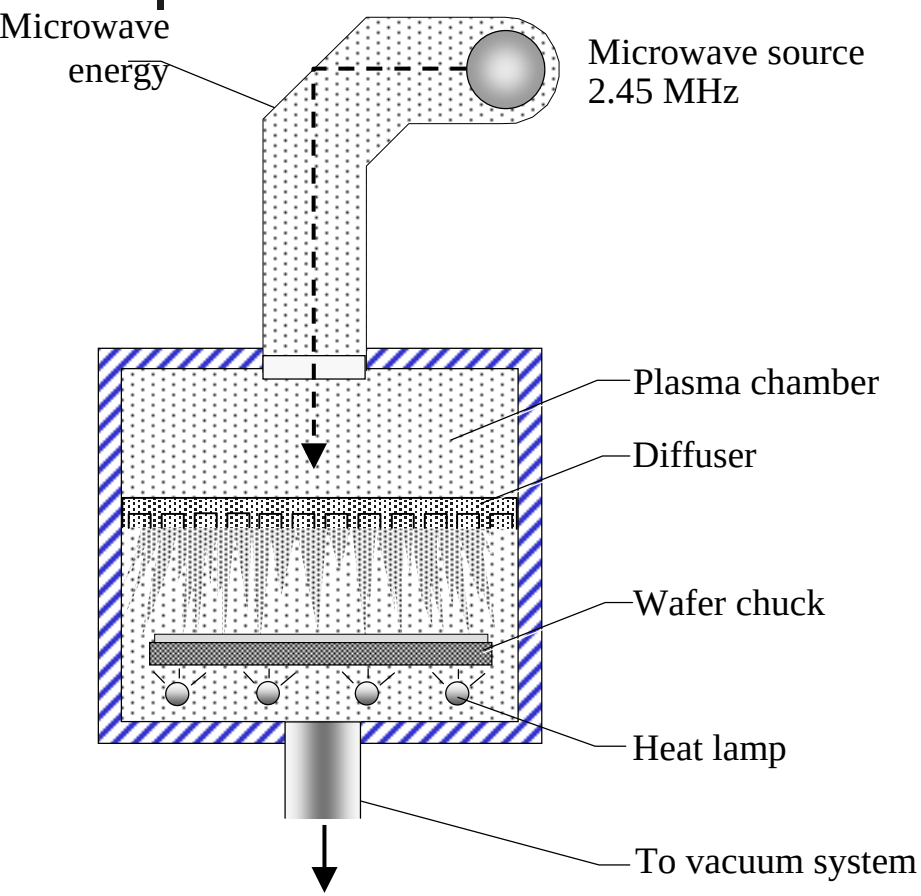
Parallel Plate Plasma Etching

Physical and chemical etch mechanisms occur in both the plasma etch mode and the RIE mode



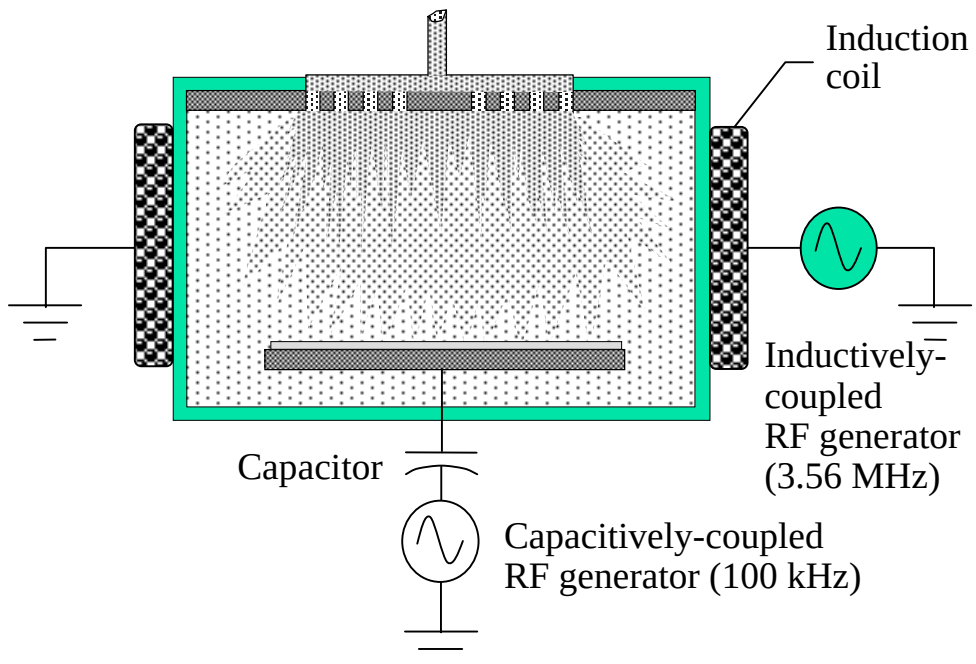
Downstream etch systems & Triode planar reactor

Downstream Reactor (remove PR)



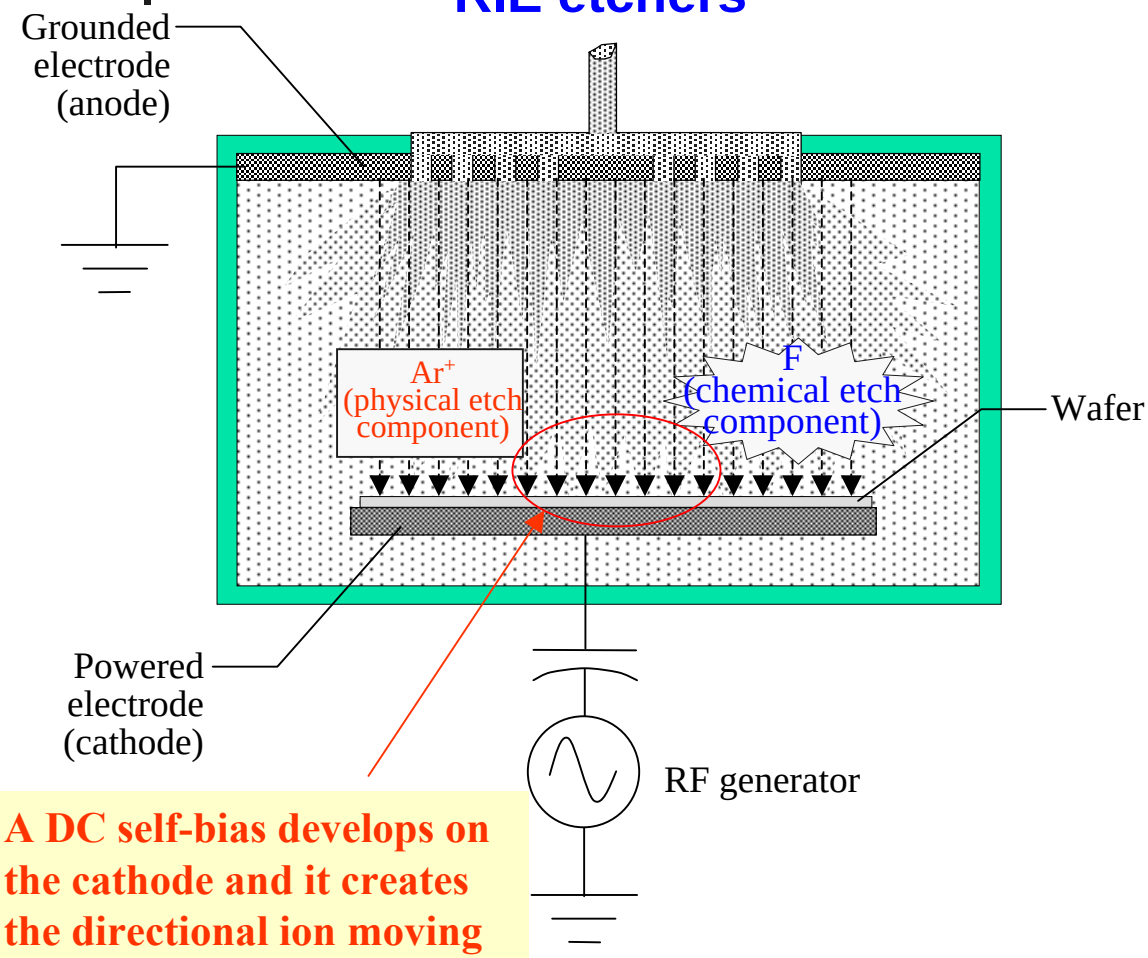
Triode Planar Reactor

Adds a third electrode to attain control over the amount of ion bombardment.



Reactive ion etch (RIE) & High-density plasma (HDP) etchers

RIE etchers

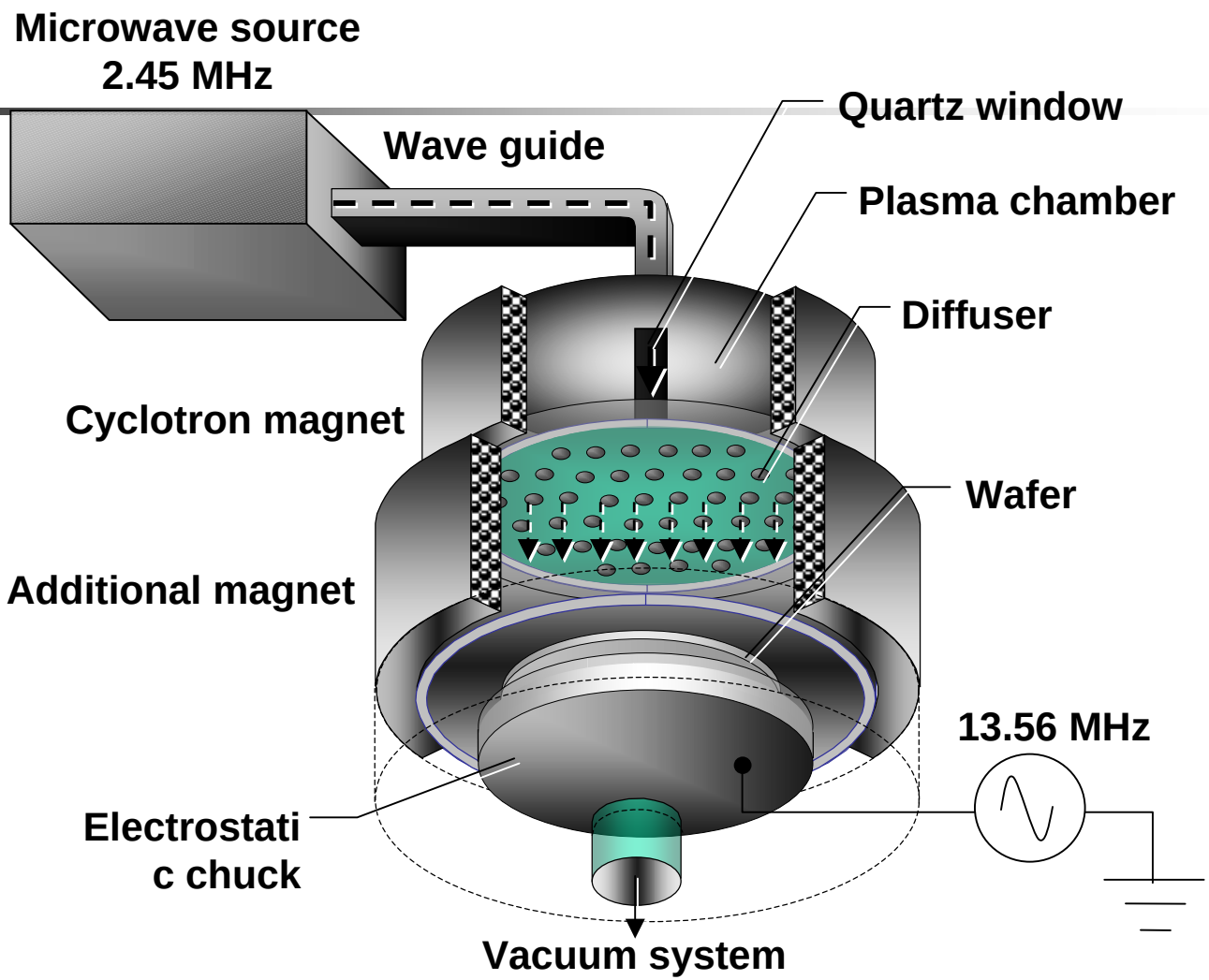


A DC self-bias develops on the cathode and it creates the directional ion moving toward wafer.

HDP Etcher

Figure 11.21 Applied Materials high-density plasma silicon etch system *(photo courtesy Applied Materials).*

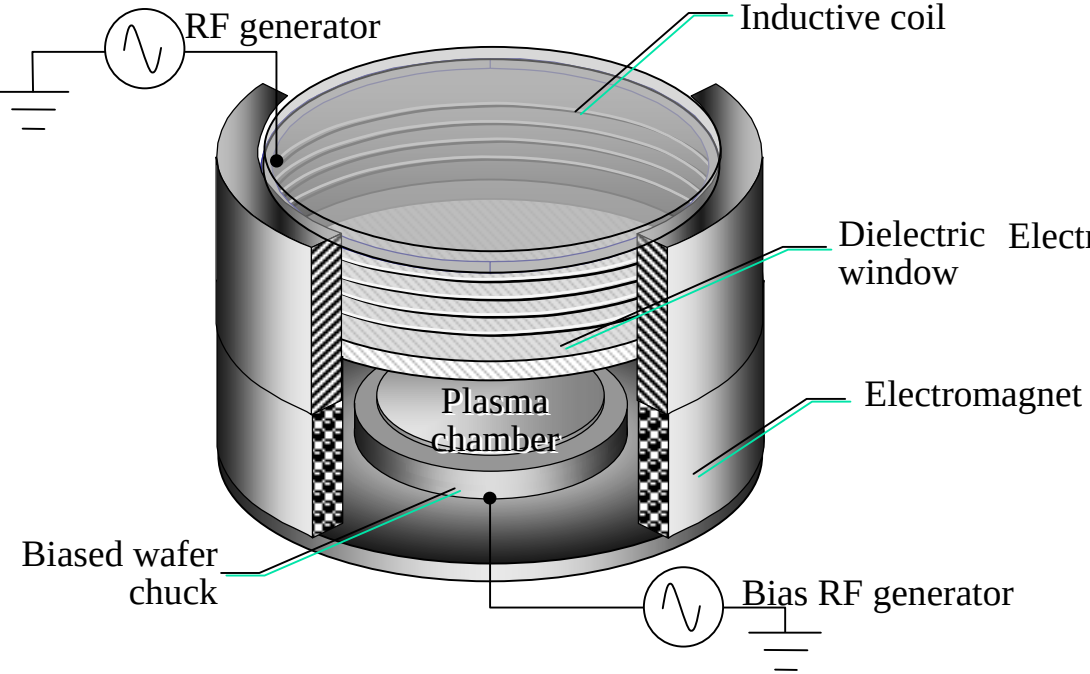
Electron Cyclotron Reactor (ECR)



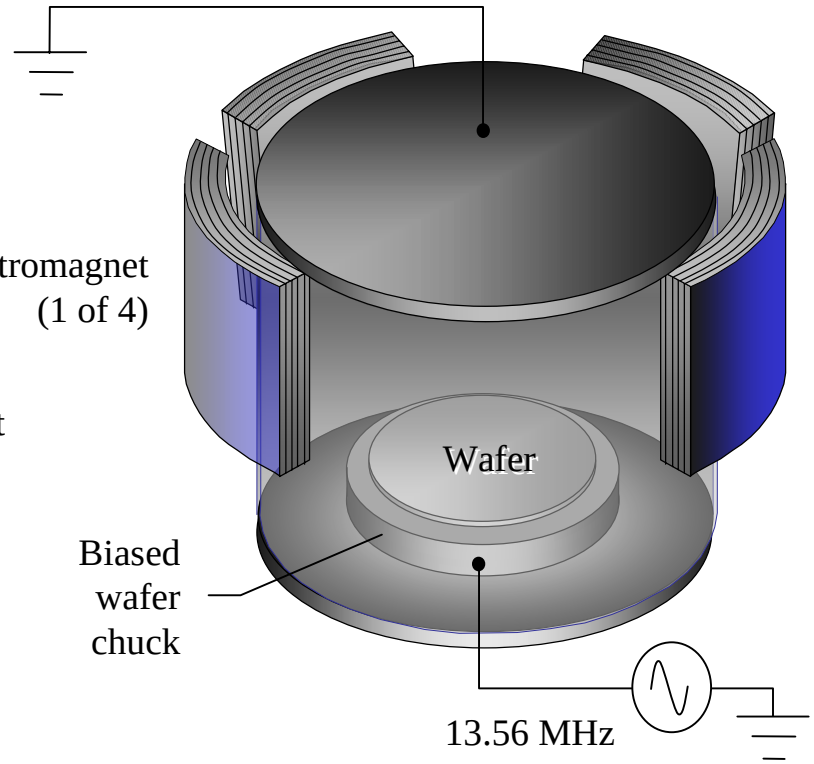
The magnetic field of ECR is parallel to the direction of reactant flow that causes free electrons to move in a spiral path due to the magnetic force → dense plasma

Inductively Coupled Plasma (ICP) & Magnetically Enhanced Reactive Ion Etch (MERIE)

ICP Etch

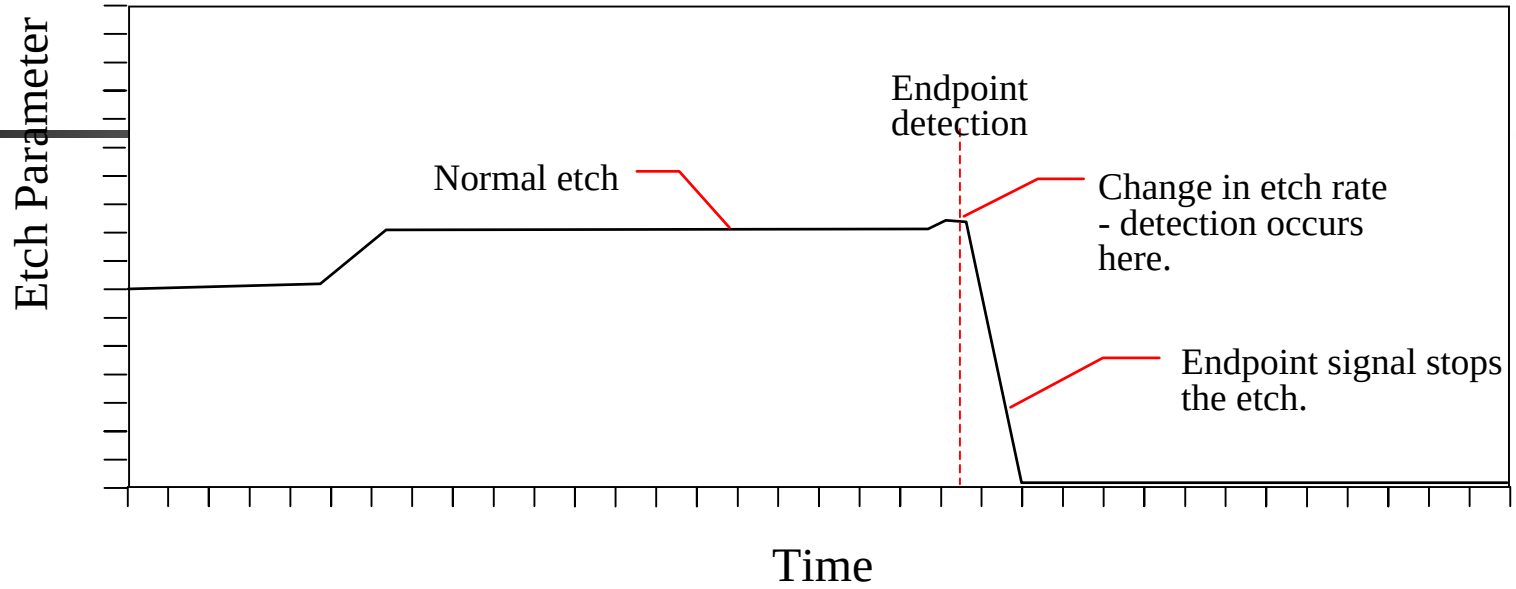


MERIE



The wafer can be biased to have both chemical and physical etching. This reactor can achieve anisotropic sidewall profiles in high-aspect ratio opening.

Endpoint Detection for Plasma Etching



Endpoint Detection

Photograph courtesy of Advanced Micro Devices, Lam Rainbow etcher

Dry Etch

Dry Etch Applications

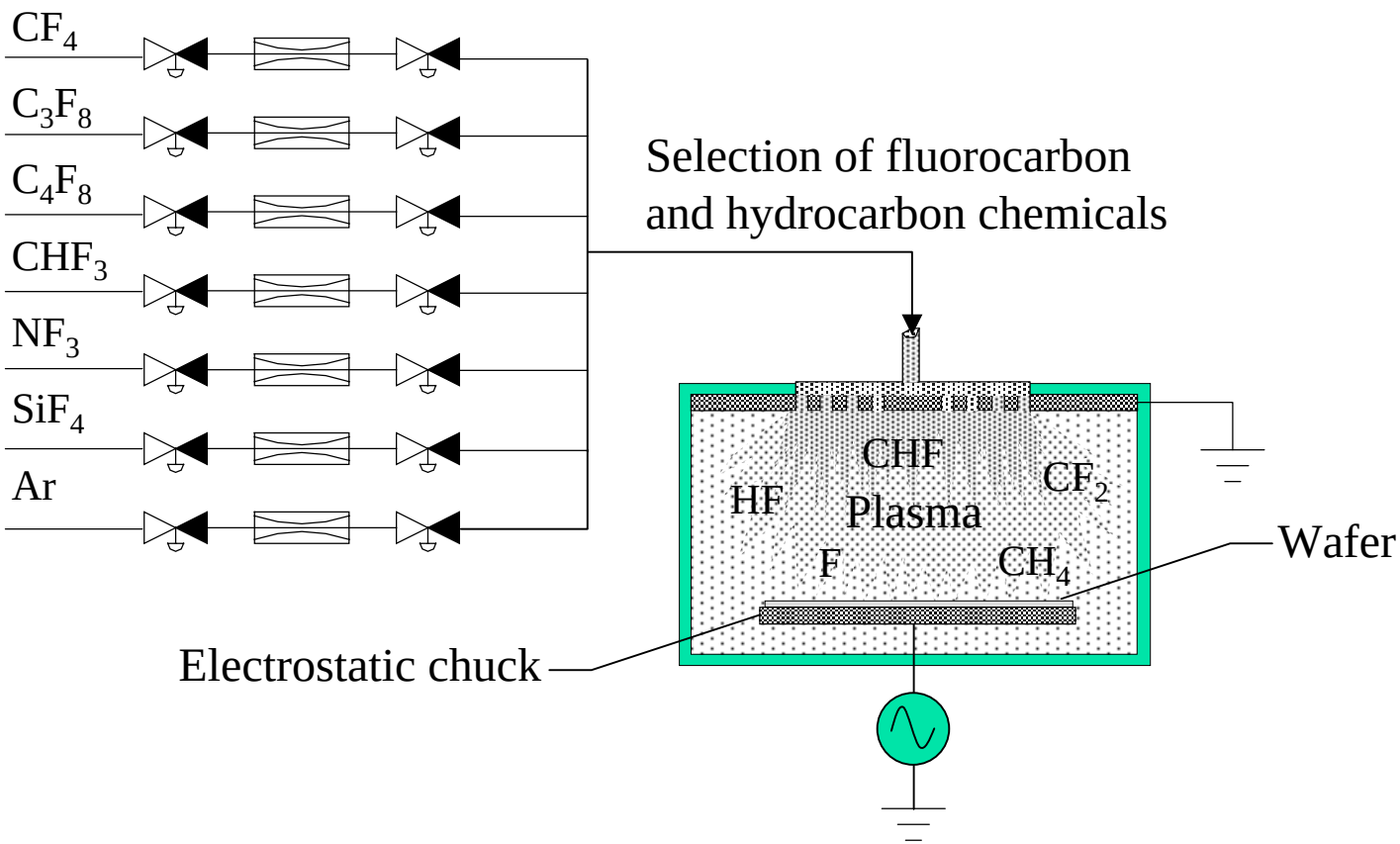
- **Dielectric Dry Etch**
  - –Oxide
  - –Silicon Nitride
- **Silicon Dry Etch**
  - –Polysilicon
  - –Single-Crystal Silicon
- **Metal Dry Etch**
  - –Aluminum and Metal Stacks
  - –Tungsten Etchback
  - –Contact Metal Etch

Requirements for Successful Dry Etch

1. **High selectivity to avoid etching materials that are not to be etched (primarily photoresist and underlying materials).**
2. **Fast etch rate to achieve an acceptable throughput of wafers.**
3. **Good sidewall profile control.**
4. **Good etch uniformity across the wafer.**
5. **Low device damage.**
6. **Wide process latitude for manufacturing.**

Dielectric Dry Etch - Oxide Etch

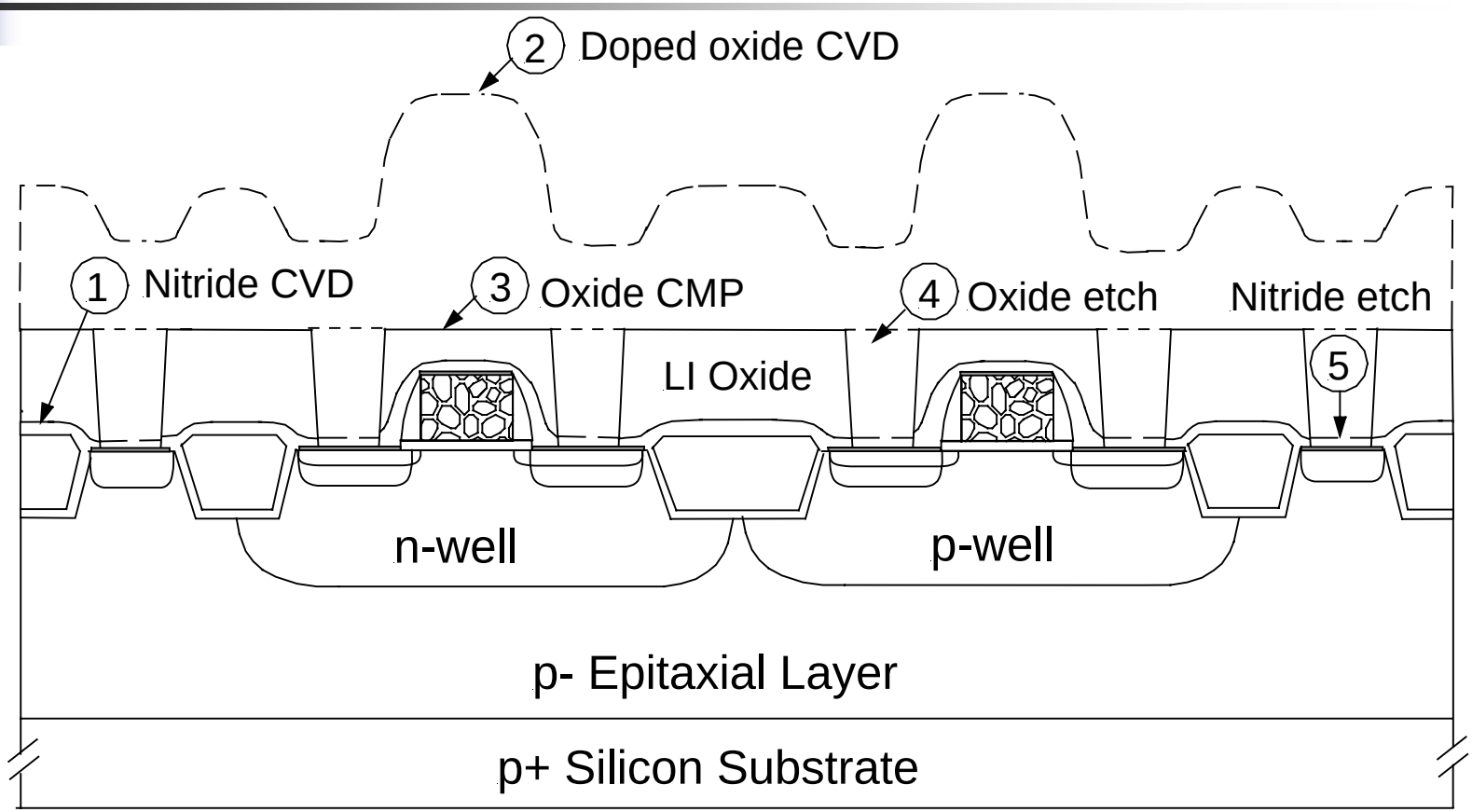
- For 0.18um DRAM : oxide etching aspect ratios = 6 : 1 ; selectivity = 50 : 1
- The oxide plasma etching process is commonly based on fluorocarbon chemistry.



Oxide Etch Reactor

Underlying Material Selectivity

Example: Silicon nitride, Si_3N_4, serves as etch-stop during LI oxide etch.
Note: The numbers show the order of the five operations.

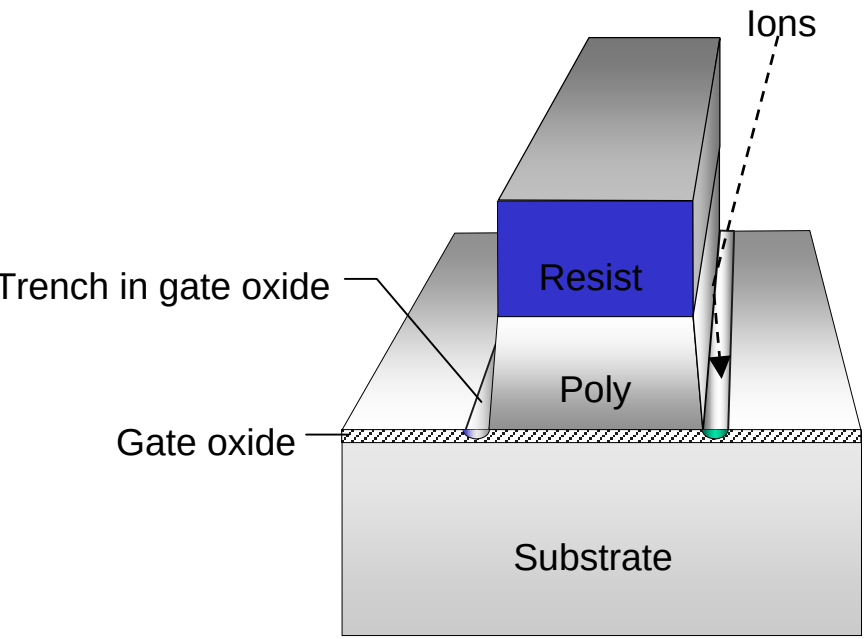


Etch Stop Hard Mask Layer

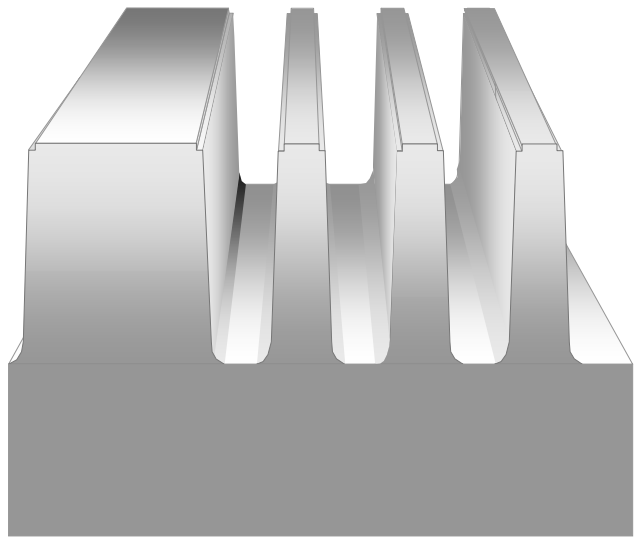
Polysilicon Gate Etch & Si Trench Etch

Polysilicon Gate Etch Process Steps:

1. **Breakthrough step to remove native oxide and surface contaminants**
2. **Main-etch step to remove most polysilicon without damage to gate oxide**
3. **Overetch step to remove remaining residues and poly stringers while maintaining high selectivity to gate oxide**



Undesirable Microtrenching during Polysilicon Gate Etching

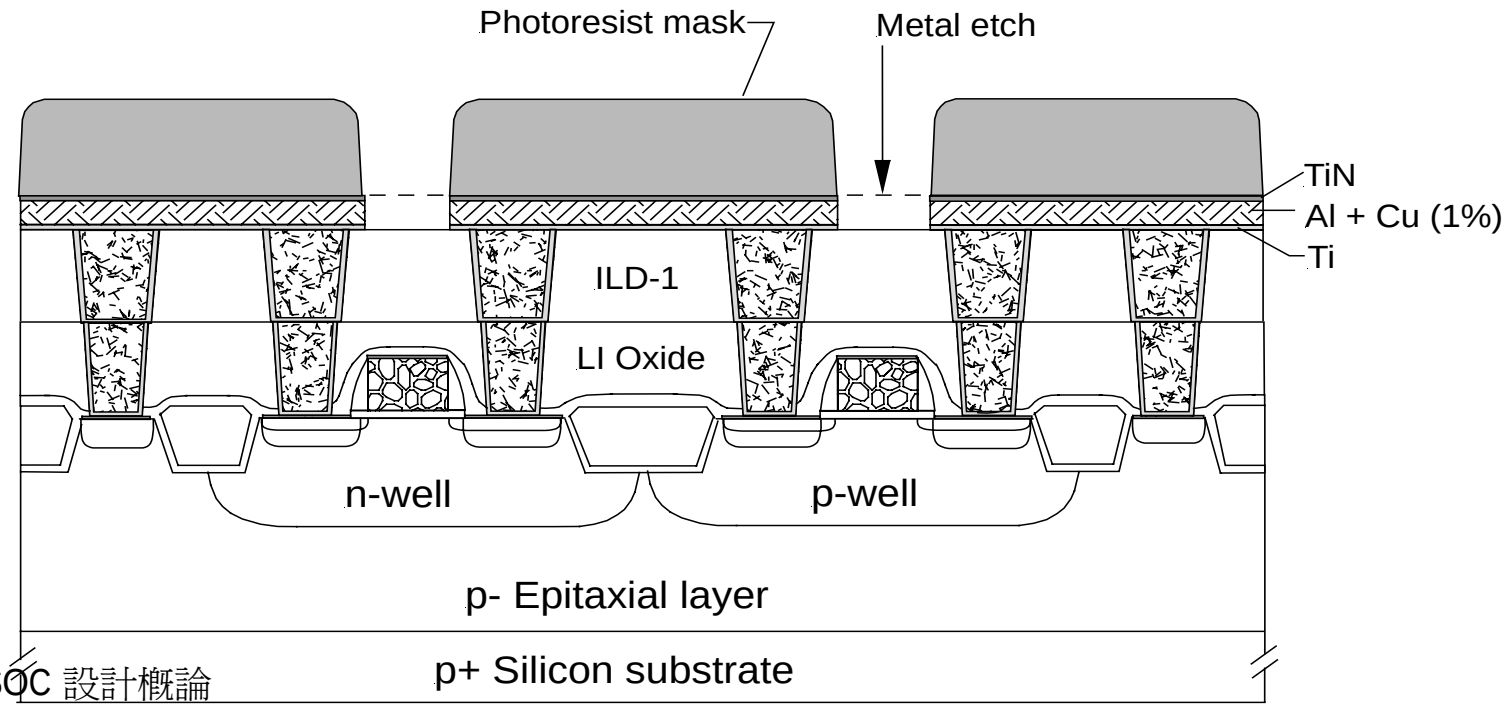


Silicon Trench Etching

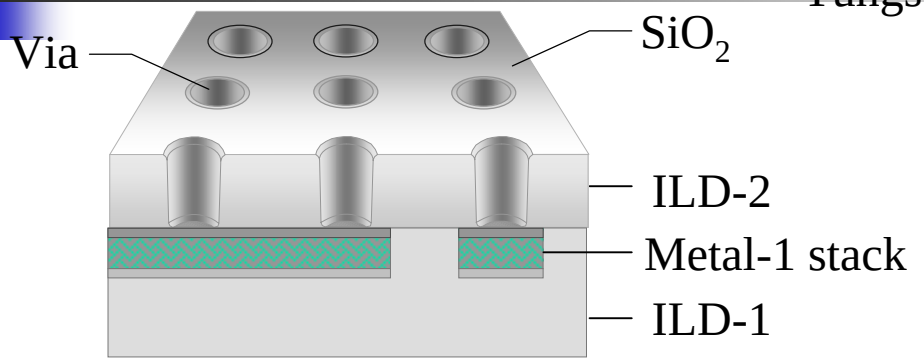
Metal Dry Etch

Typical Steps for Etching Metal Stacks

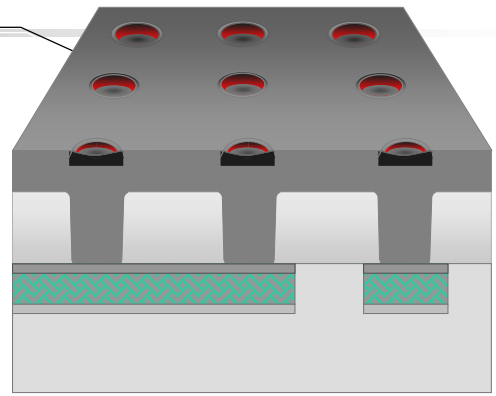
1. **Breakthrough step to remove native oxide.**
2. **ARC layer etch (may be combined with above step).**
3. **Main etch step of aluminum.**
4. **Overetch step to remove residue. It may be a continuation of main etch step.**
5. **Barrier layer etch.**
6. **Optional residue removal process to prevent corrosion.**
7. **Resist removal.**



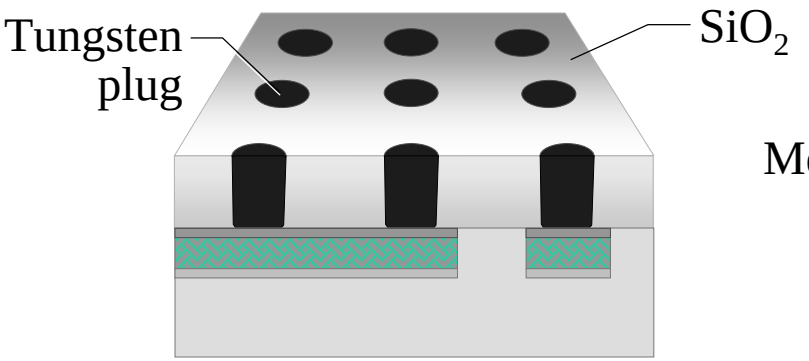
Metal Dry Etch - Tungsten Etchback



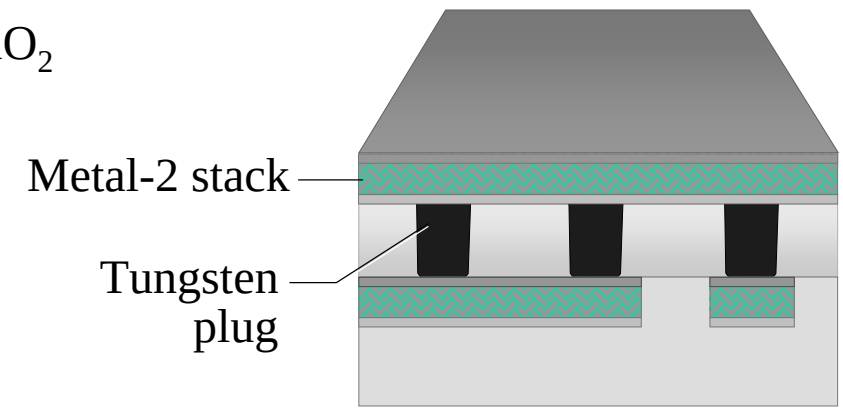
(a) Via etch through ILD-2 (SiO2)



(b) Tungsten CVD via fill



(c) Tungsten etchback



(d) Metal-2 deposition

Wet Etch

Parameter	Explanation	Difficulty to Control
Concentration	Solution concentration (e.g., ratio of NH4F:HF for etch an oxide).	Most difficult parameter to control because the bath concentration is continually changing.
Time	Time of wafer immersion in the wet chemical bath.	Relatively easy to control.
Temperature	Temperature of wet chemical bath.	Relatively easy to control.
Agitation	Agitation of the solution bath.	Moderate difficulty to properly control.

Wet Etch Parameters

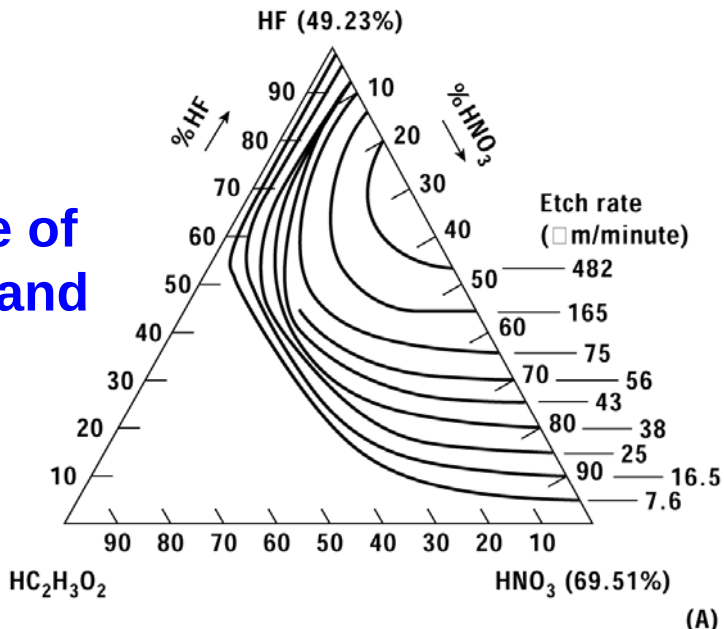
Wet Etch Rate of Oxide and Silicon

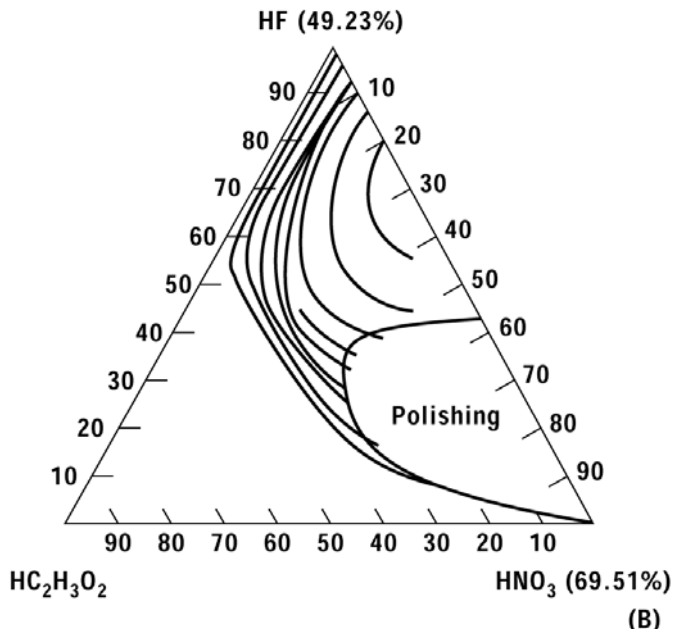
Approximate Oxide Etch Rates in BHF Solution at 25° C

Table 16.8[1] Approximate Oxide Etch Rates in BHF Solution at 25°C[a]		
Type of Oxide	**Density (g/cm^3)**	**Etch Rate (nm/s)**
Dry grown	2.24 – 2.27	1
Wet grown	2.18 – 2.21	1.5
CVD deposited	< 2.00	1.5[b] – 5[c]
Sputtered	< 2.00	10 – 20

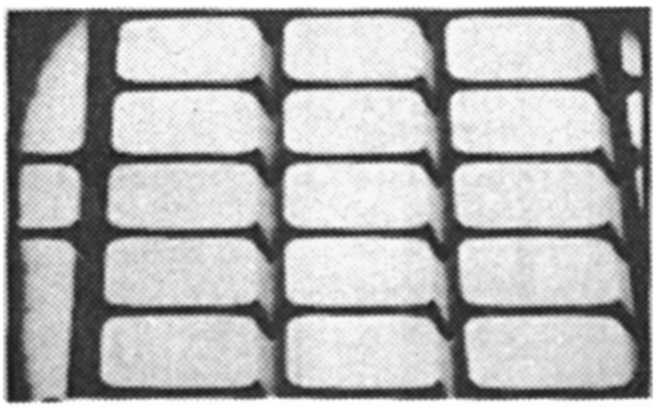
a) 10 parts of 454 g NH_4F in 680 ml H_2O and one part 48% HF
b) Annealed at approximately 1000°C for 10 minutes
c) Not annealed

The Etch Rate of Silicon in HF and HNO_3



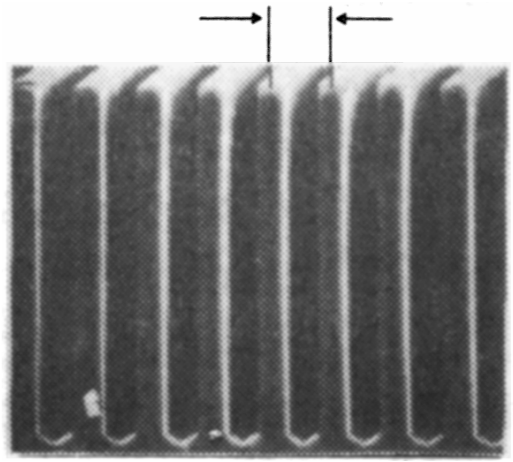


Wet Anisotropic Etching



SEM TOP VIEW (100) DI ETCH

SEM CROSSECTIONAL VIEW (100) DI ETCH



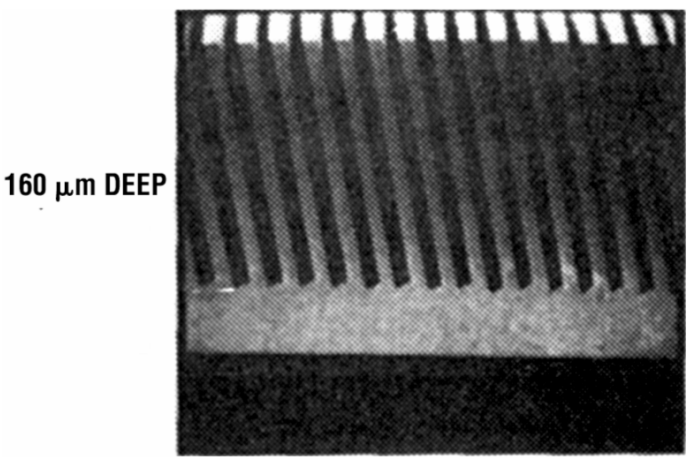


Figure 11.6 (100) silicon wafers after directional etching in KOH, isopropyl alcohol, and water. The upper photo shows a 50-mm-deep etch. The lower photographs are of 80-mm-deep trenches etched at 10 mm pitch on (110) and 107 off (110) *(after Bean, ©1978 IEEE).*

Photoresist Removal
Atomic Oxygen Reaction with Resist in Asher