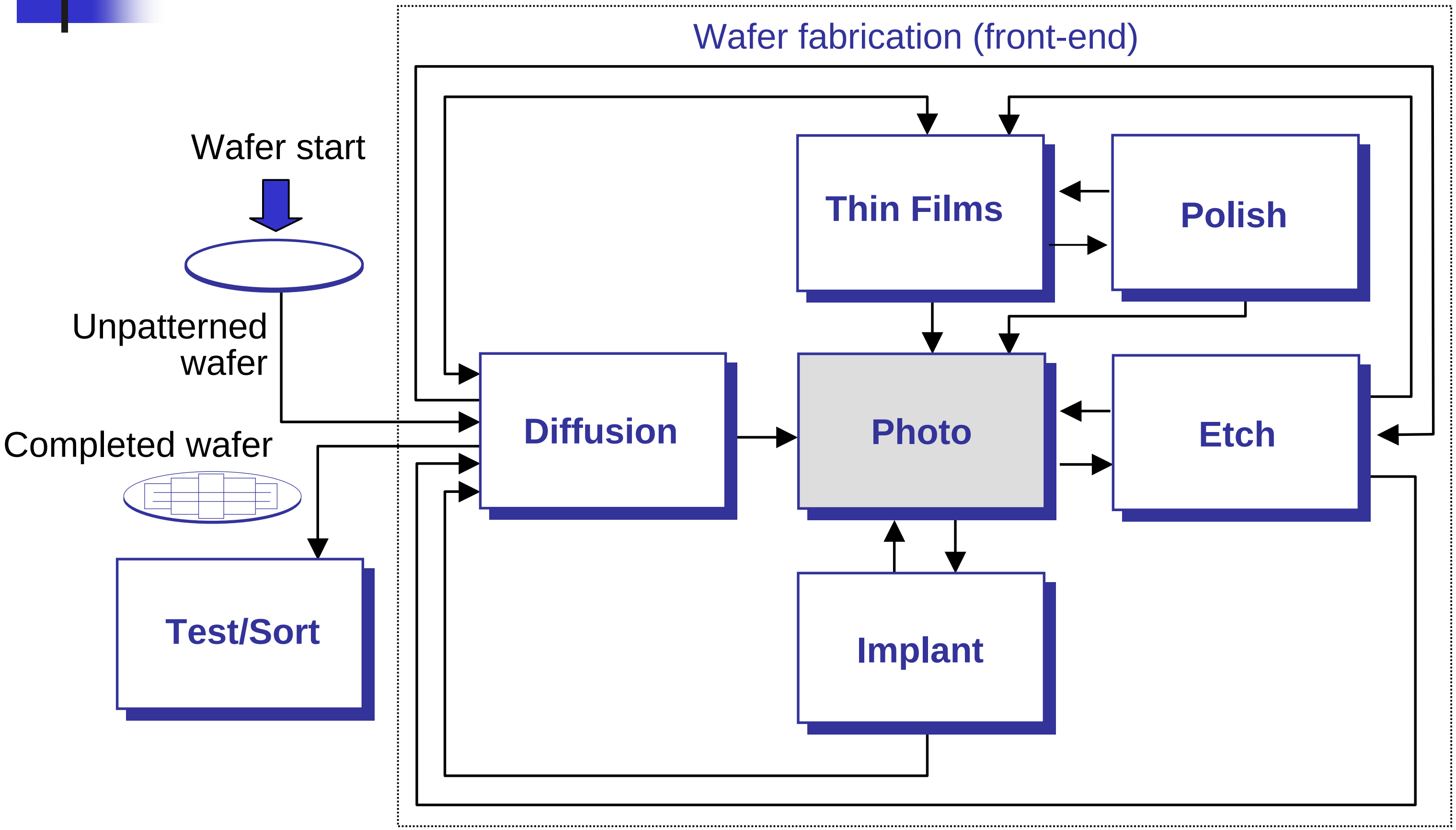
Chapter 3 : ULSI Manufacturing Technology
- (c) Photolithography

Reference

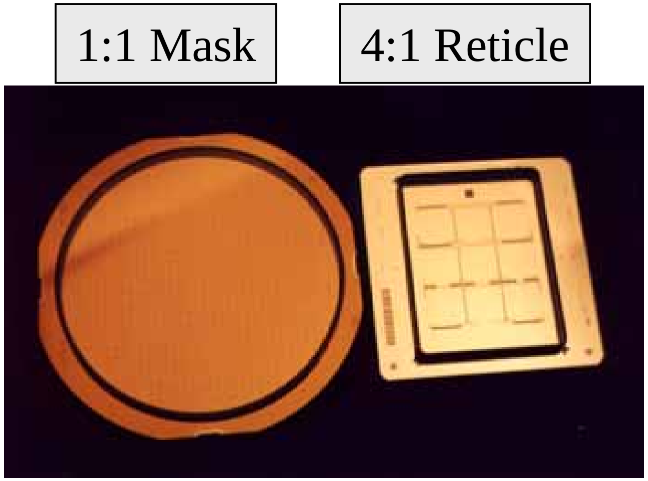
1. Semiconductor Manufacturing Technology
   : Michael Quirk and Julian Serda (2001)
2. 國家矽導計畫-教育部晶片法商學程教材 (2004)
3. Semiconductor Physics and Devices- Basic Principles(3/e)
   : Donald A. Neamen (2003)
4. Semiconductor Devices - Physics and Technology (2/e)
   : S. M. Sze (2002)
5. ULSI Technology *: C. Y. Chang, S. M. Sze (1996)*

Photolithography

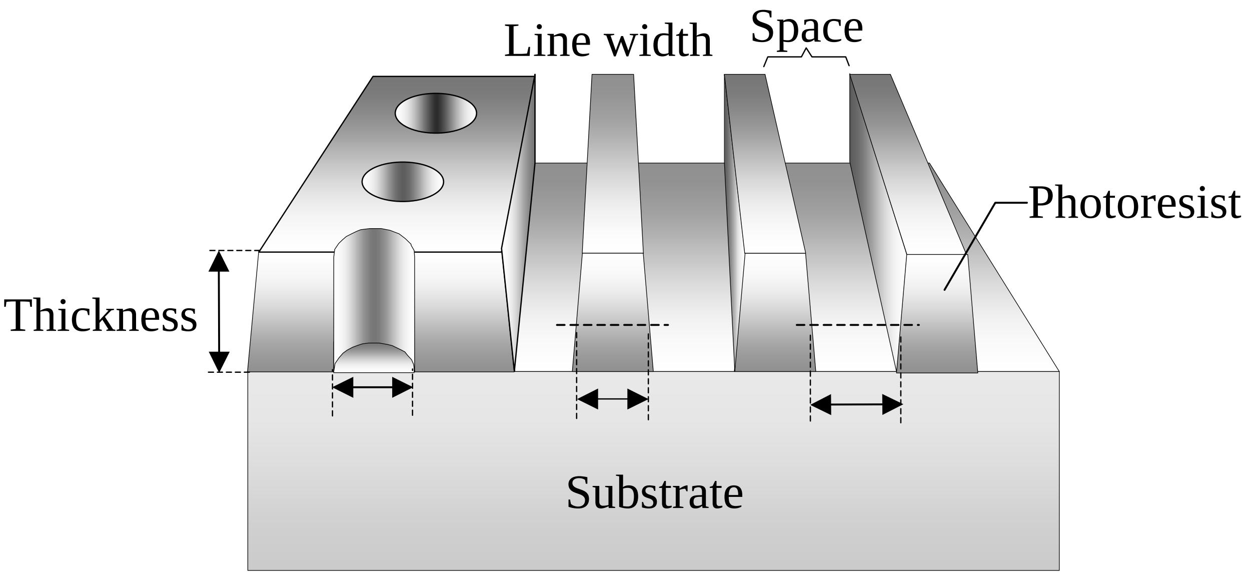


Wafer Fabrication Process Flow

Photolithography Concepts



1. Photomask and Reticle for Microlithography

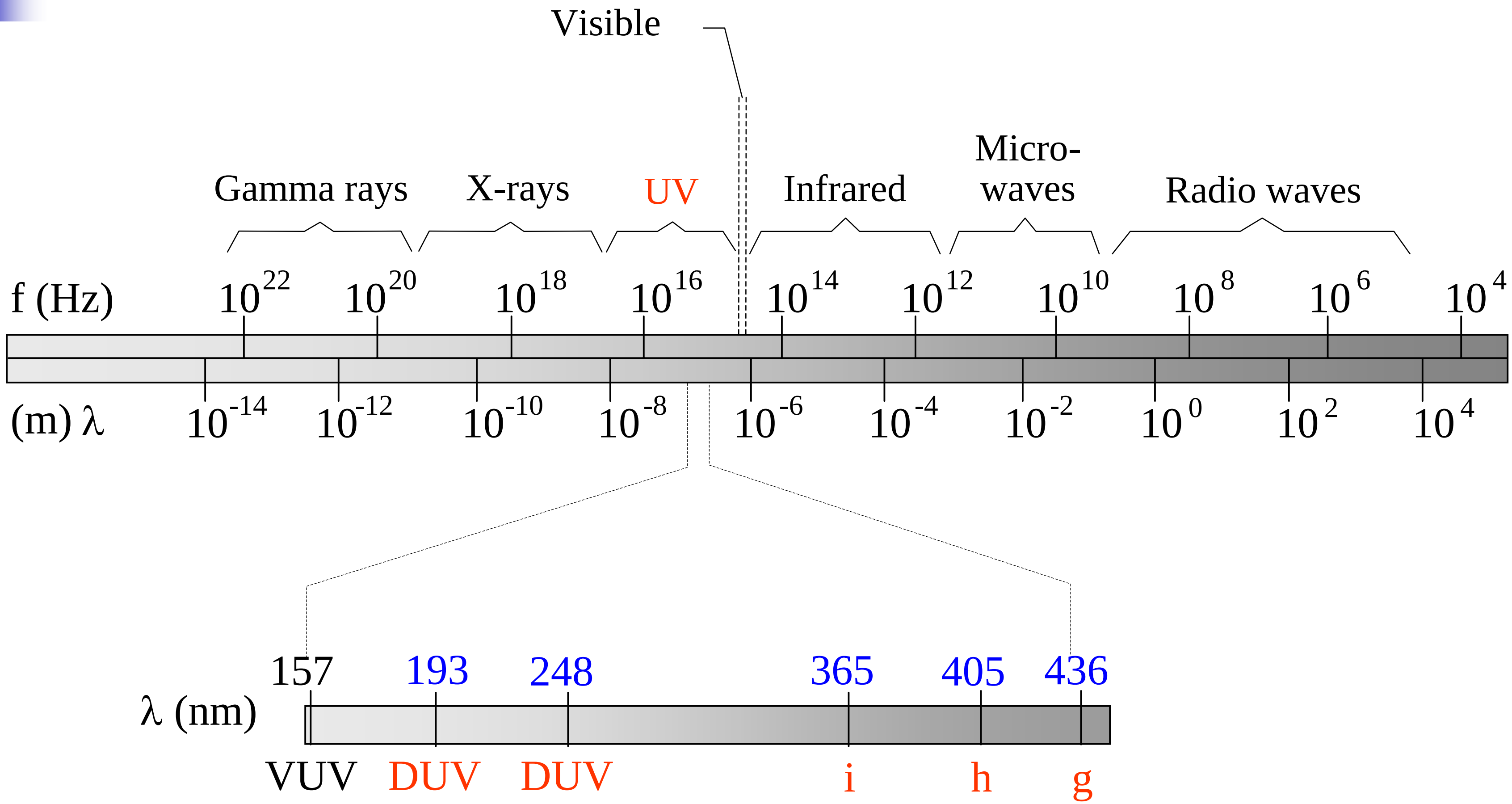


2. Three Dimensional Pattern in Photoresist (CD:critical dimension)

Photolithography Concepts

3. Light Spectrum & Resolution

(a) Section of the Electromagnetic Spectrum



Common UV wavelengths used in optical lithography.

Photolithography Concepts

3. Light Spectrum & Resolution

(b) Important Wavelengths for Photolithography Exposure

UV Wavelength (nm)	Wavelength Name	UV Emission Source
436	g-line	Mercury arc lamp
405	h-line	Mercury arc lamp
365	i-line	Mercury arc lamp
248	Deep UV (DUV)	Mercury arc lamp or Krypton Fluoride (KrF) excimer laser
193	Deep UV (DUV)	Argon Fluoride (ArF) excimer laser
157	Vacuum UV (VUV)	Fluorine (F_2) excimer laser

Photolithography Concepts

4. Importance of Mask Overlay Accuracy

The masking layers determine the accuracy by which subsequent processes can be performed.

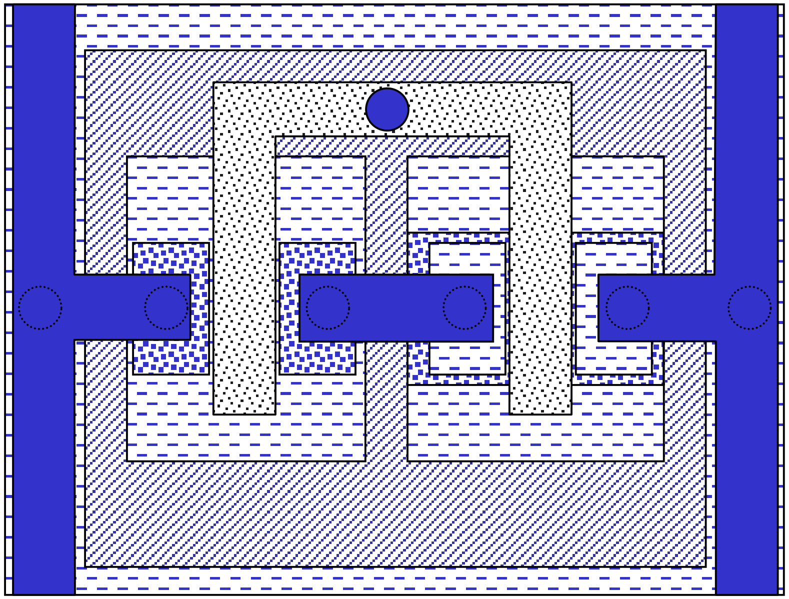
Different types overlay misalignment affect the overlay budget. Misalignment is caused by poor alignment between the mask and the wafer.

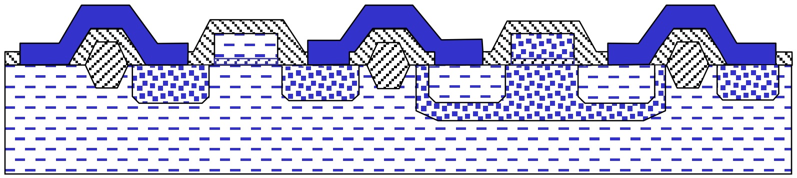
The photoresist mask pattern prepares individual layers for proper placement, orientation, and size of structures to be etched or implanted.

A large overlay budget essentially reduces the circuit density, which limits device feature sizes and, therefore, IC performance.

Small sizes and low tolerances do not provide much room for error.

Top view of CMOS inverter



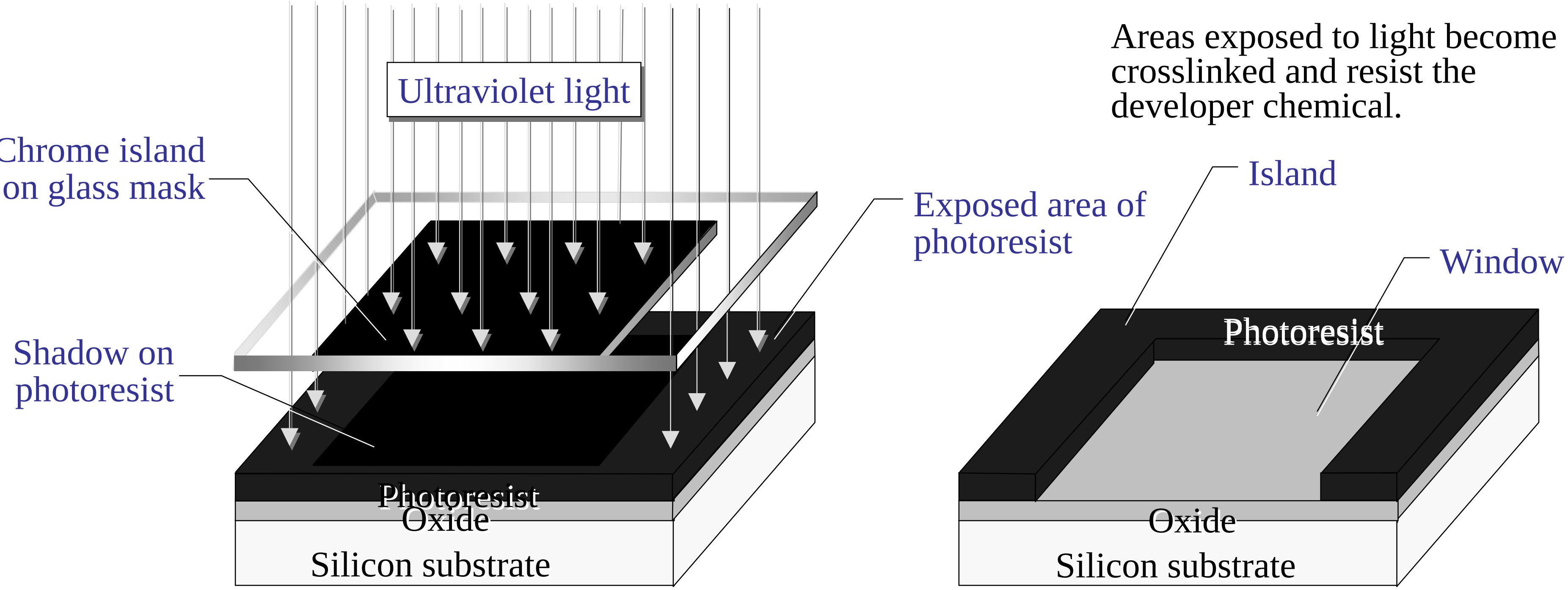


Cross section of CMOS inverter

Photolithography Concepts

5. Photolithography Processes

(a) Negative Lithography



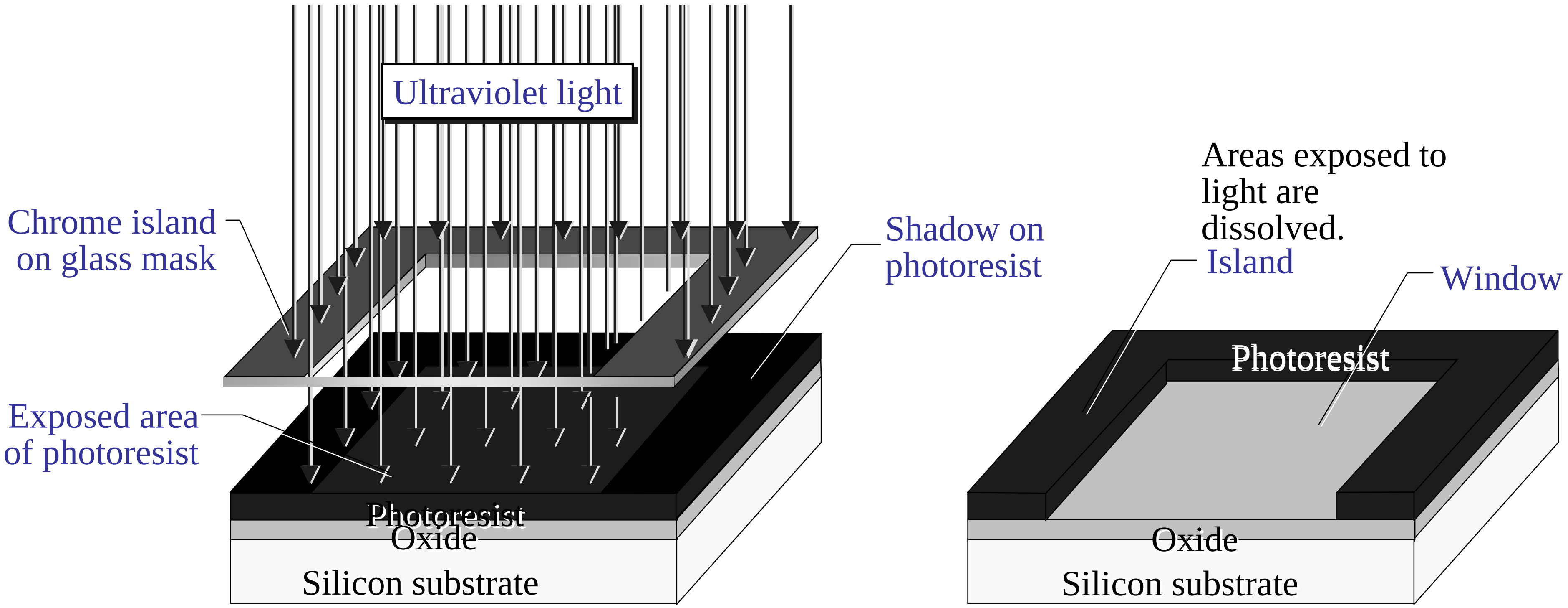
Areas exposed to light become crosslinked and resist the developer chemical.

Resulting pattern after the resist is developed.

Photolithography Concepts

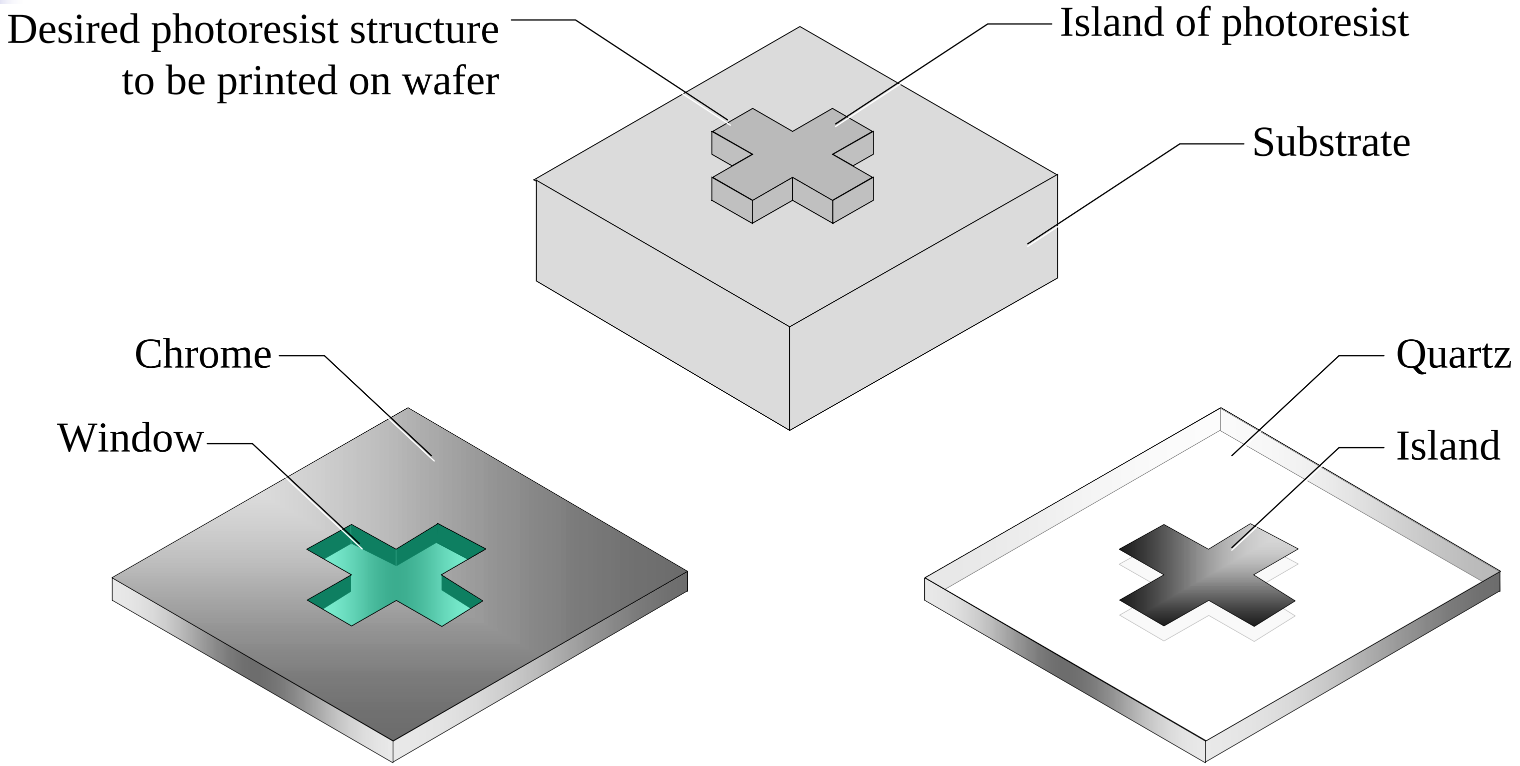
5. Photolithography Processes

(b) Positive Lithography



Resulting pattern after the resist is developed.

Relationship Between Mask and Resist



Desired photoresist structure
to be printed on wafer

Island of photoresist

Substrate

Chrome

Window

Quartz

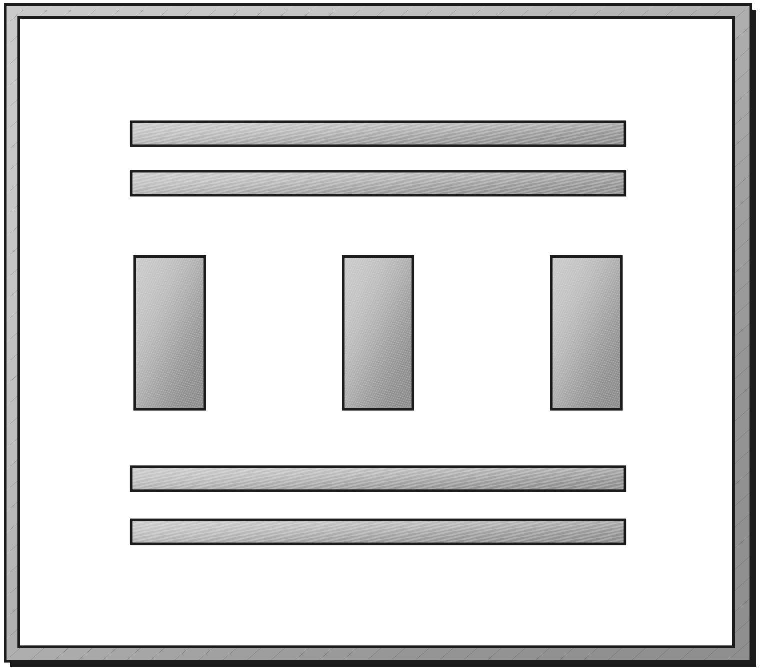
Island

Mask pattern required when
using negative photoresist
(opposite of intended structure)

Mask pattern required when
using positive photoresist
(same as intended structure)

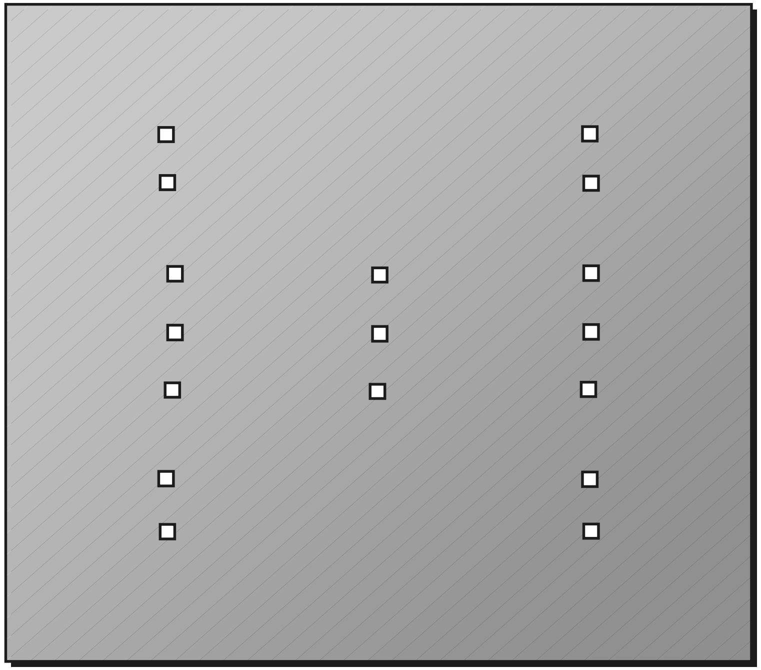
Clear Field and Dark Field Masks

Clear Field Mask



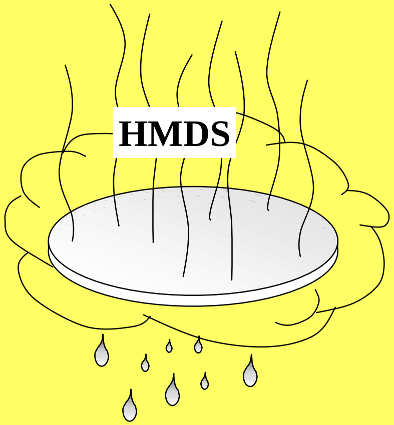
Simulation of metal interconnect lines (positive resist lithography)

Dark Field Mask

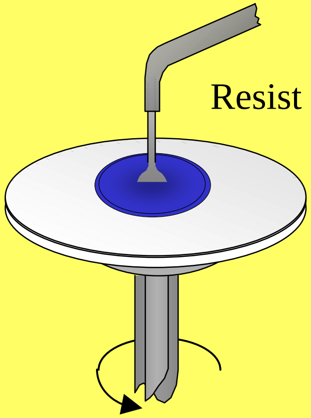


Simulation of contact holes (positive resist lithography)

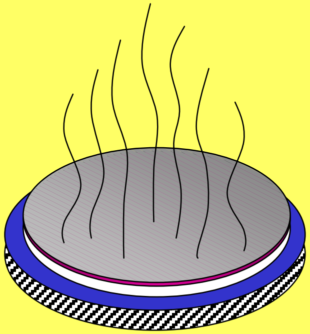
Eight Steps of Photolithography



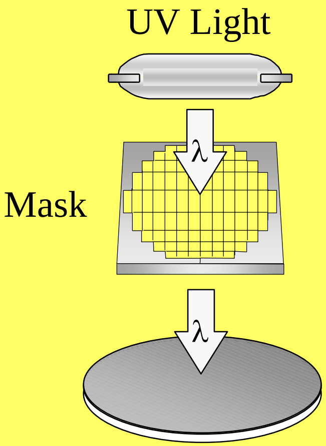
1) Vapor prime



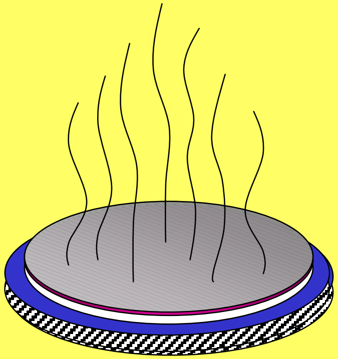
2) Spin coat



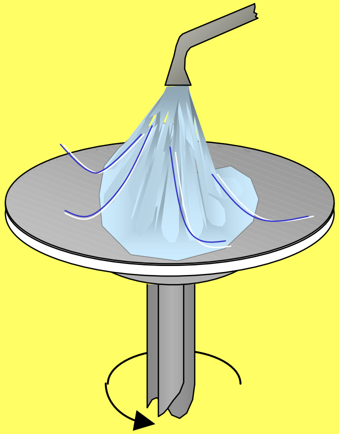
3) Soft bake



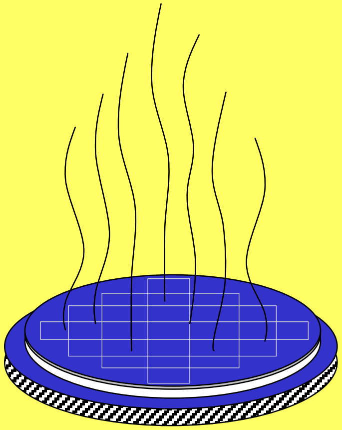
4) Alignment and Exposure



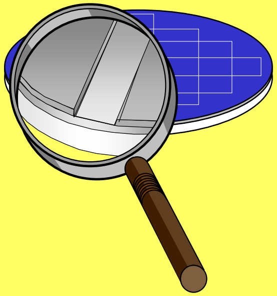
5) Post-exposure bake



6) Develop

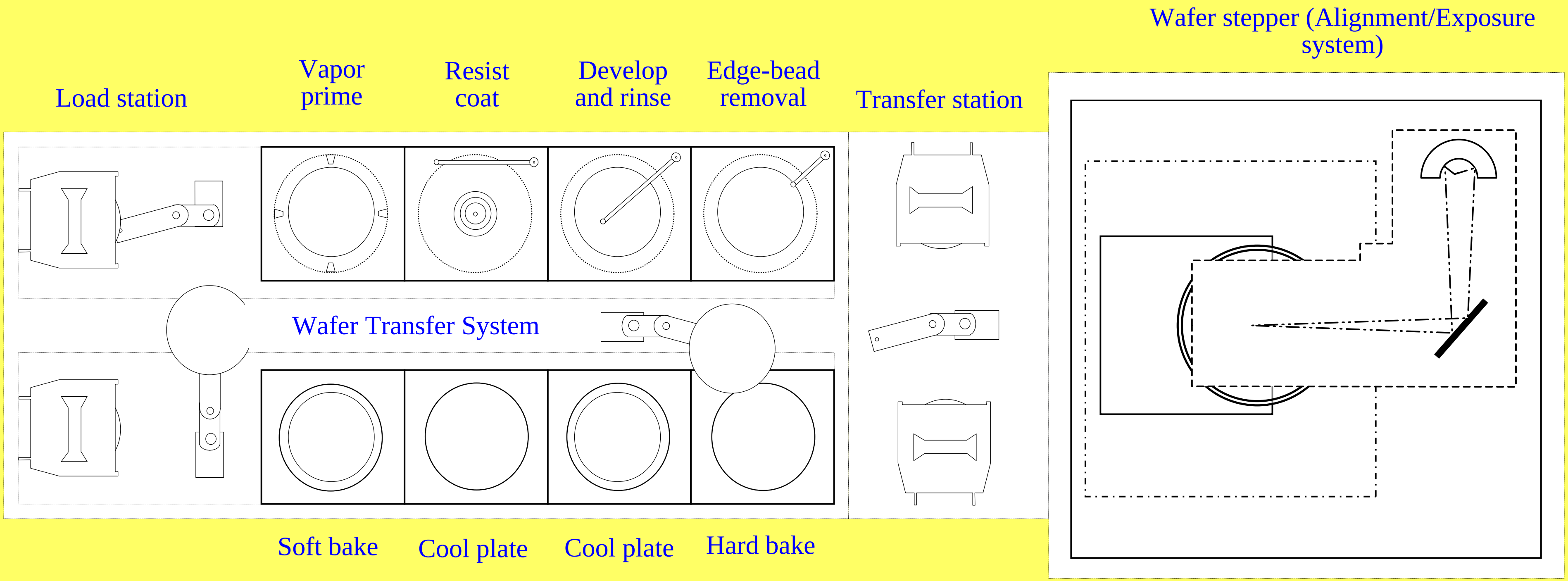


7) Hard bake



8) Develop inspect

Automated Wafer Track for Photolithography



Wafer stepper (Alignment/Exposure system)

Load station

Vapor prime

Resist coat

Develop and rinse

Edge-bead removal

Transfer station

Wafer Transfer System

Soft bake

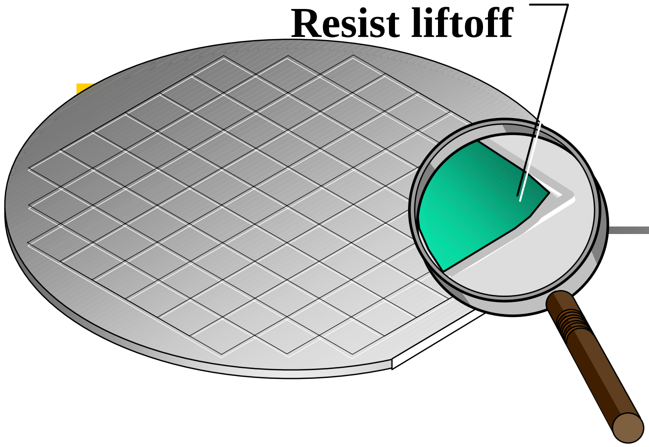
Cool plate

Cool plate

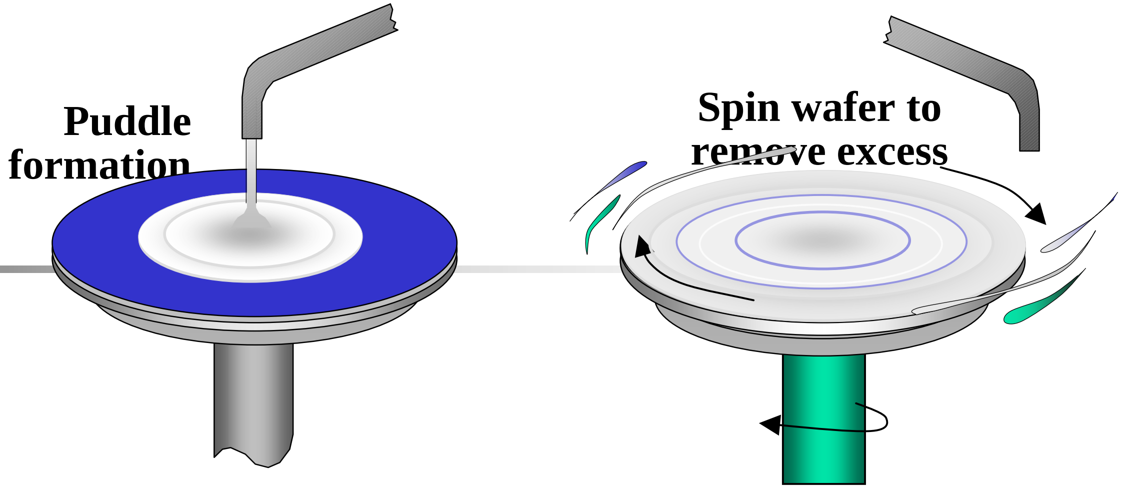
Hard bake

Photo courtesy of Advanced Micro Devices, TEL Track Mark VIII

1. Vapor Prime

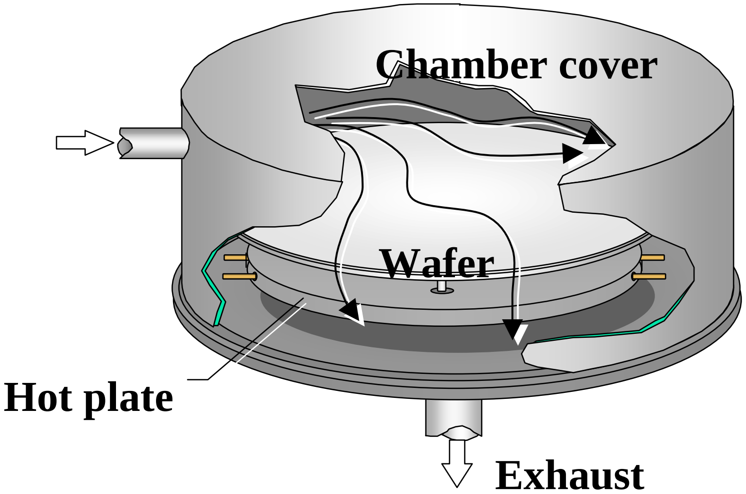


Effect of Poor Resist Adhesion Due to Surface Contamination



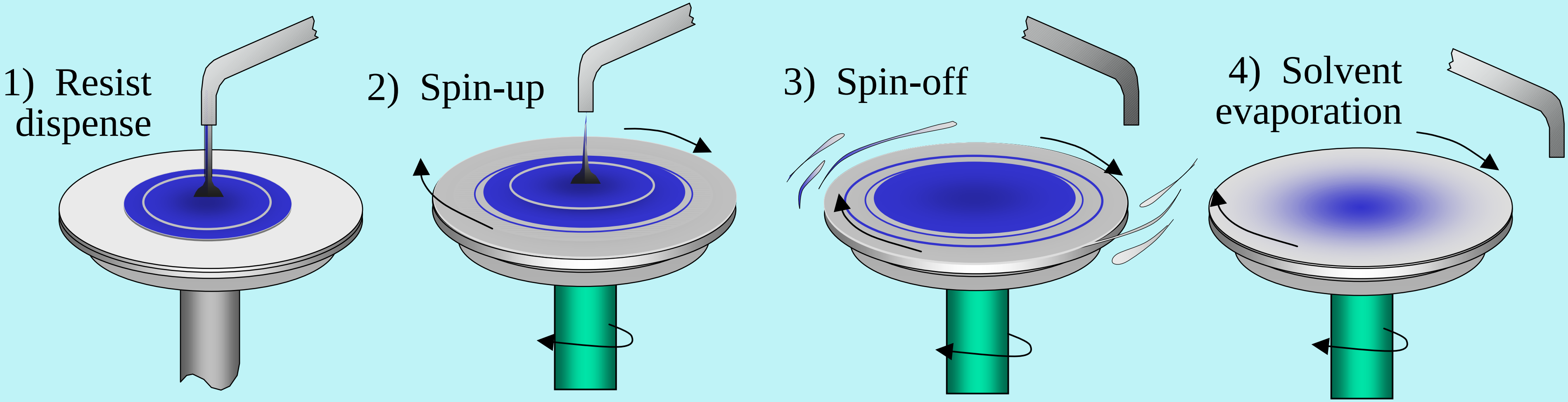
HMDS Puddle Dispense and Spin

- **Promotes Good Photoresist-to-Wafer Adhesion**
- **Primes Wafer with Hexamethyldisilazane, HMDS**
- **Followed by Dehydration Bake**
- **Ensures Wafer Surface is Clean and Dry**



HMDS Hot Plate Dehydration Bake and Vapor Prime

2. Spin Coat



<u>Process Summary</u>:

Wafer is held onto vacuum chuck

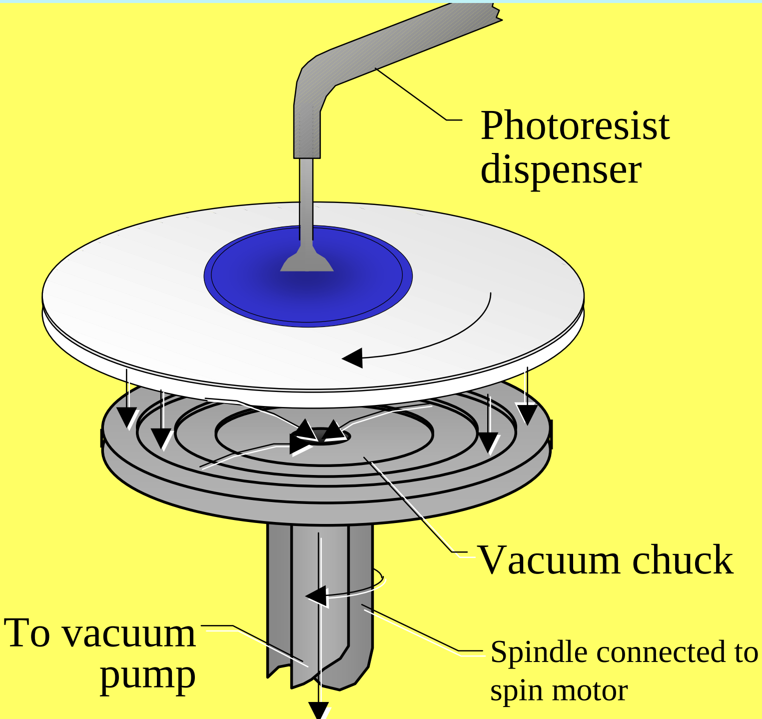
Dispense ~5ml of photoresist

Slow spin ~ 500 rpm

Ramp up to ~ 3000 to 5000 rpm

Quality measures:

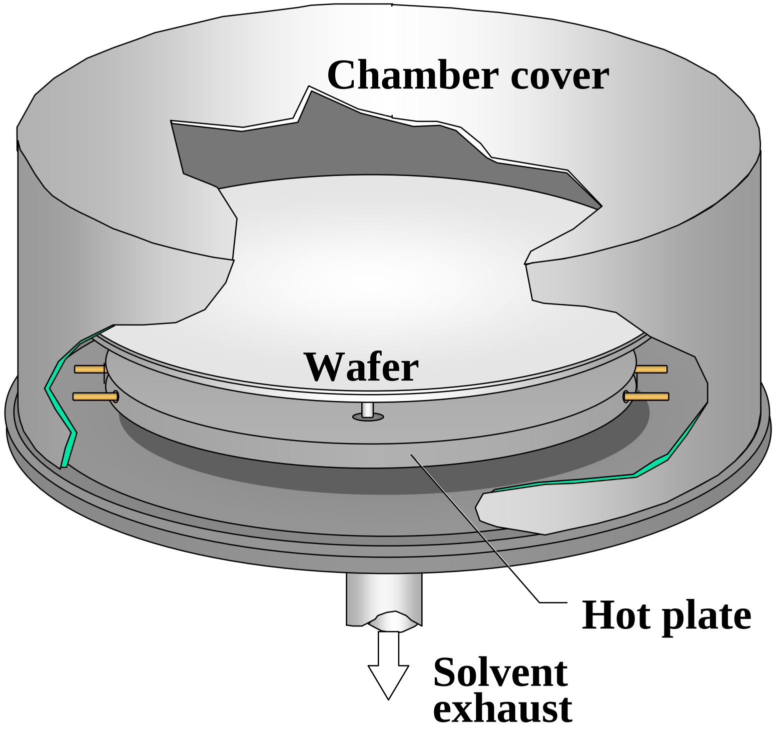
- time
- speed
- thickness
- uniformity
- particles and defects



3. Soft bake

Characteristics of Soft Bake:

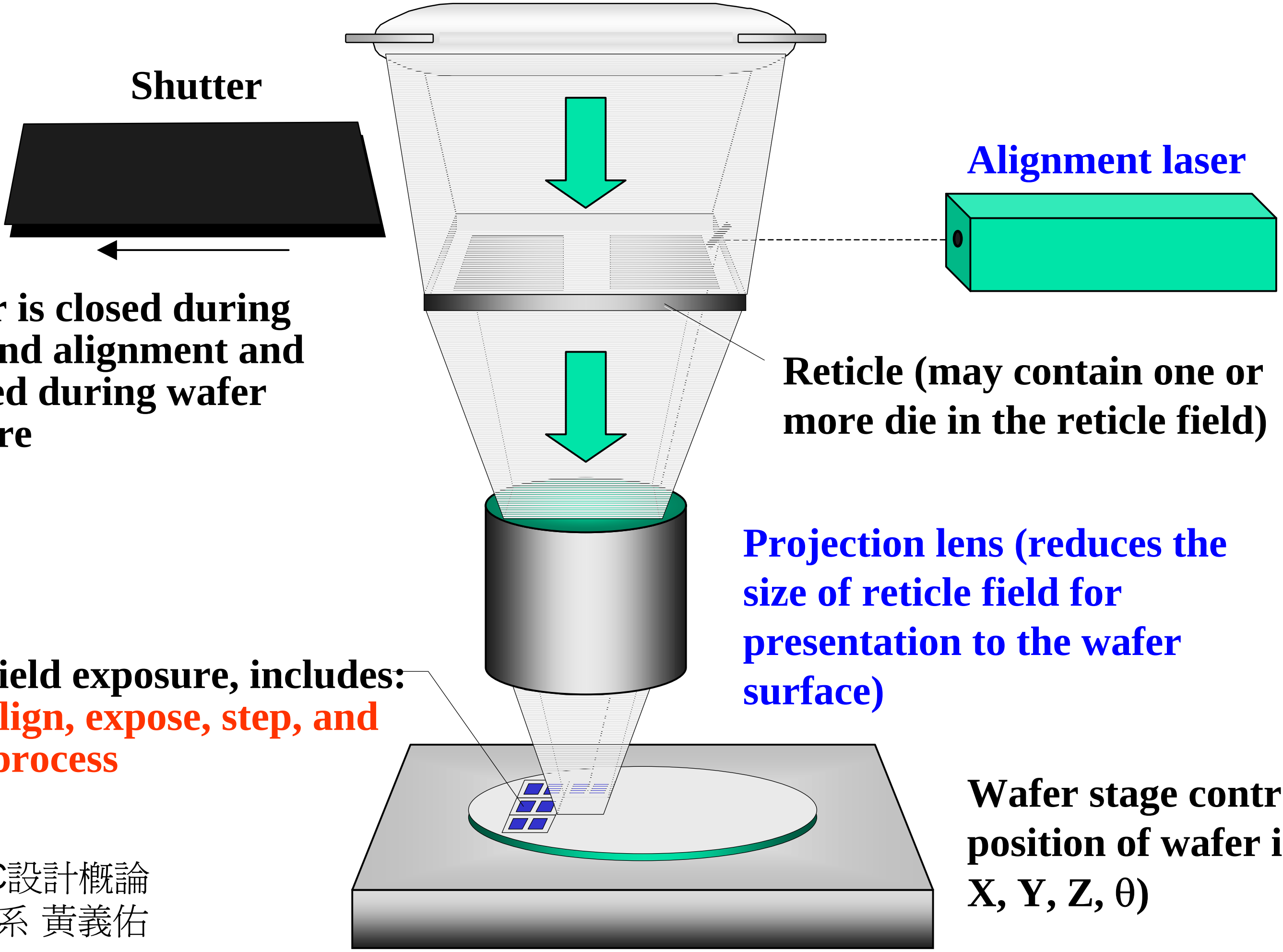
- **Improves Photoresist-to-Wafer Adhesion**
- **Promotes Resist Uniformity on Wafer**
- **Improves Line width Control During Etch**
- **Drives Off Most of Solvent in Photoresist**
- **Typical Bake Temperatures are 90 to 100°C**
  - **For About 30 Seconds**
  - **On a Hot Plate**
  - **Followed by Cooling Step on Cold Plate**



Soft Bake on Vacuum Hot Plate

4. Alignment and Exposure

Reticle Pattern Transfer to Resist



UV light source

Shutter

Shutter is closed during focus and alignment and removed during wafer exposure

Alignment laser

Reticle (may contain one or more die in the reticle field)

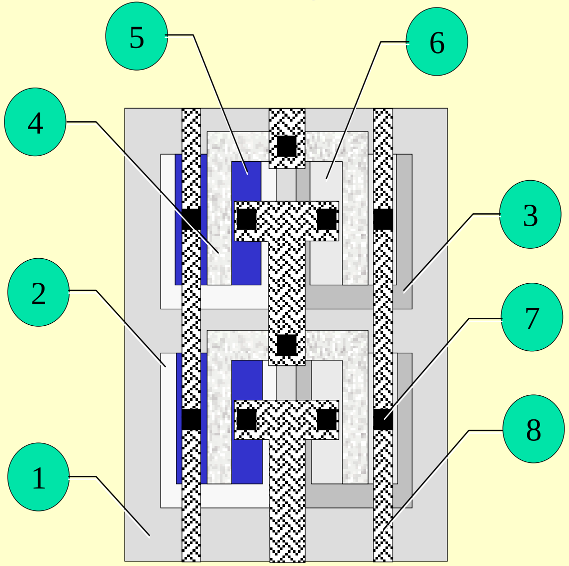
Projection lens (reduces the size of reticle field for presentation to the wafer surface)

Single field exposure, includes: focus, align, expose, step, and repeat process

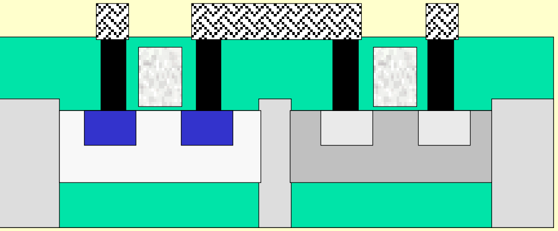
Wafer stage controls position of wafer in X, Y, Z, θ)

Layout and Dimensions of Reticle Patterns

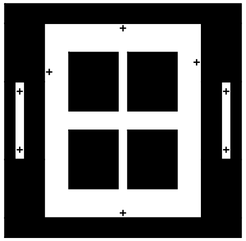
Resulting layers



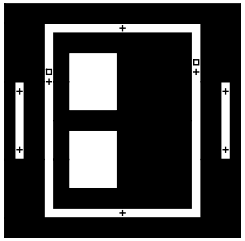
Top view



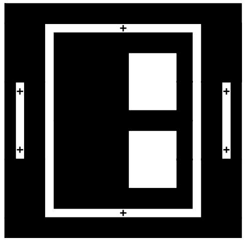
Cross section



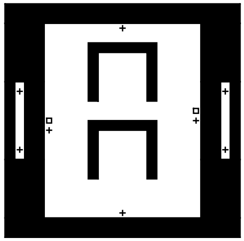
1) STI etch



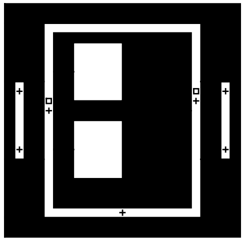
2) P-well implant



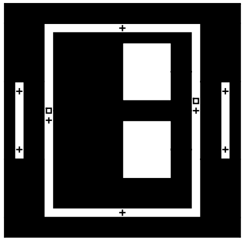
3) N-well implant



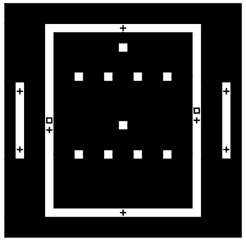
4) Poly gate etch



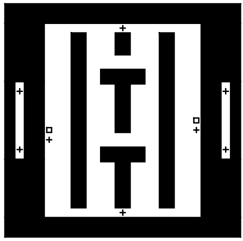
5) N^+ S/D implant



6) P^+ S/D implant



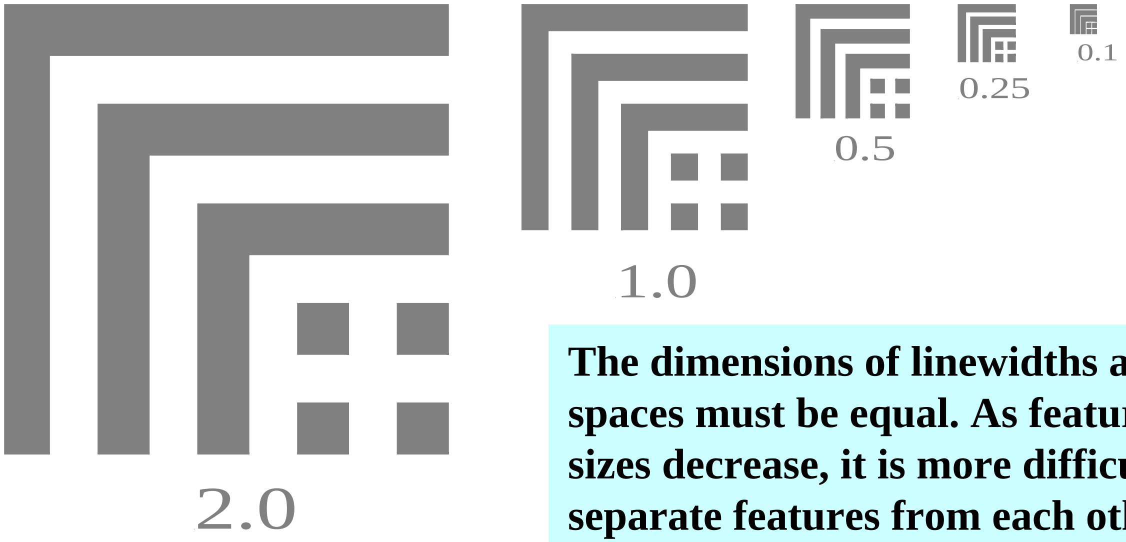
7) Oxide contact etch



8) Metal etch

Optics- Resolution of Features

k = process factor that represents specific applications (0.6~0.8)
NA = numerical aperture of the exposure system



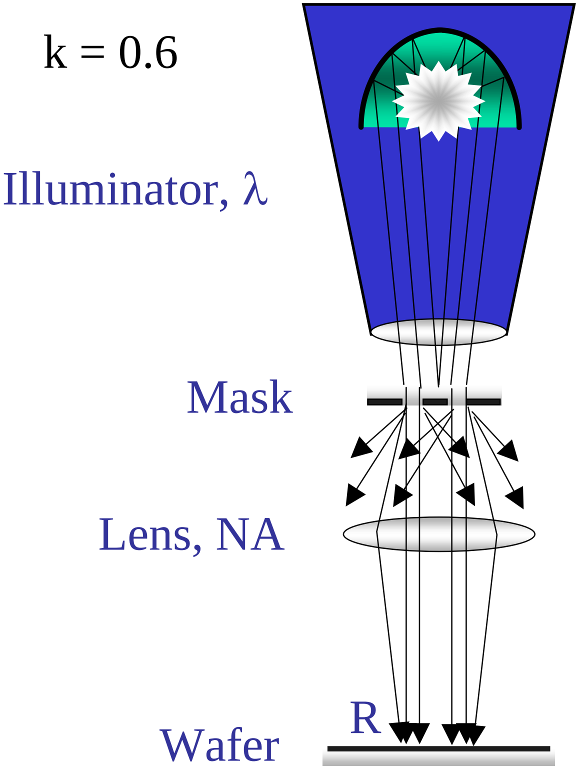
The dimensions of linewidths and spaces must be equal. As feature sizes decrease, it is more difficult to separate features from each other.

$$R = \frac{k\,\lambda}{NA}$$

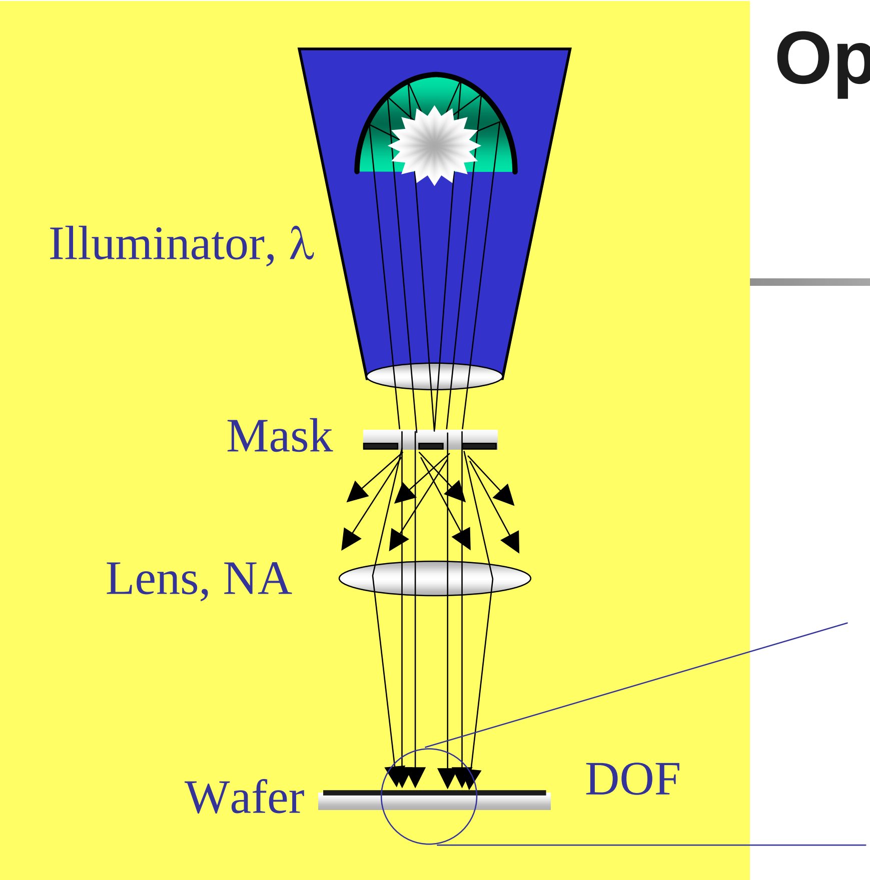
	λ	NA	R
i-line	365 nm	0.45	486 nm
	365 nm	0.60	365 nm
DUV	193 nm	0.45	257 nm
	193 nm	0.60	193 nm

Calculating Resolution for a given λ, NA and k

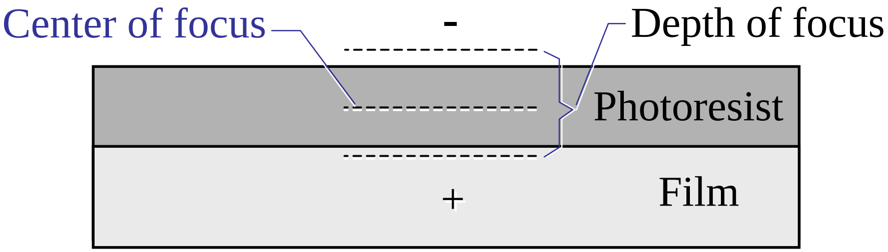
k = 0.6



Optics - Depth of Focus (DOF)



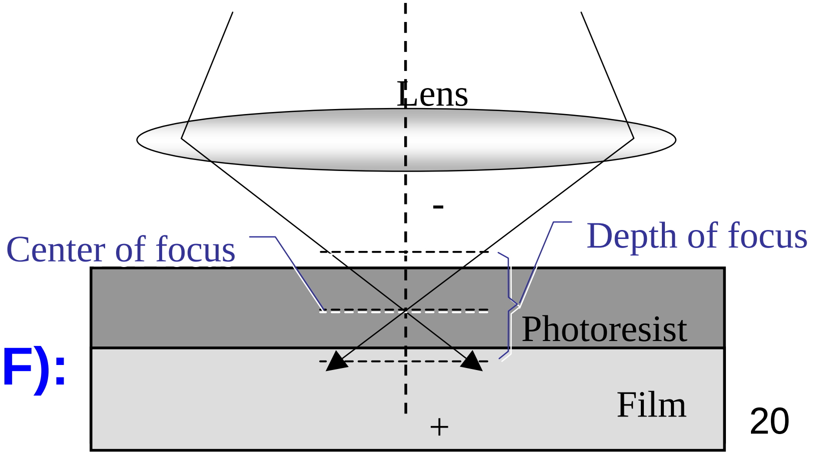
	λ	NA	R	DOF
i-line	365 nm	0.45	486 nm	901 nm
	365 nm	0.60	365 nm	507 nm
DUV	193 nm	0.45	257 nm	476 nm
	193 nm	0.60	193 nm	268 nm



Resolution Versus Depth of Focus for Varying NA

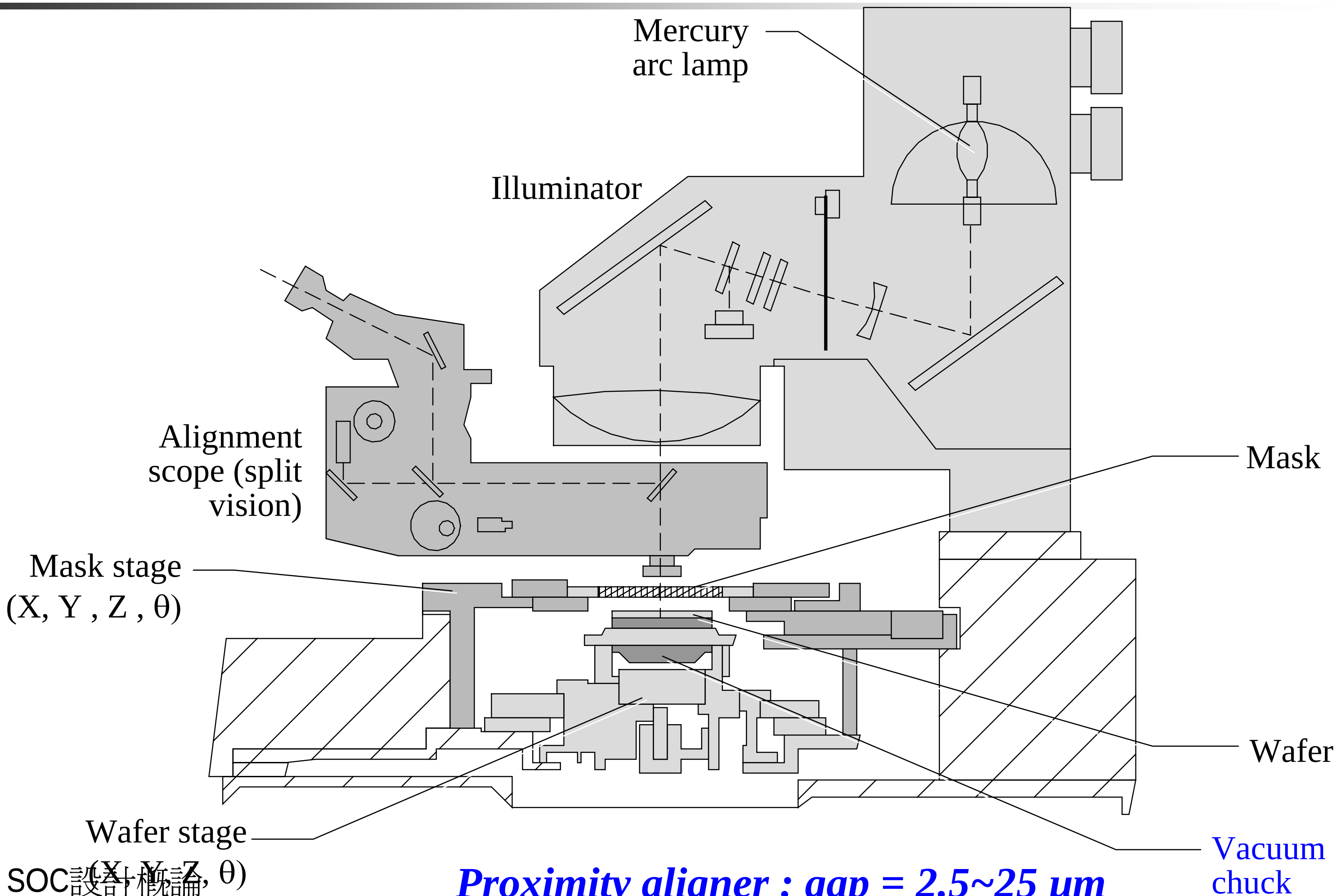
$$\text{DOF} = \frac{\lambda}{2(\text{NA})^2}$$

Depth of Focus (DOF):



Photolithography Equipment

(a) Contact / Proximity Aligner System

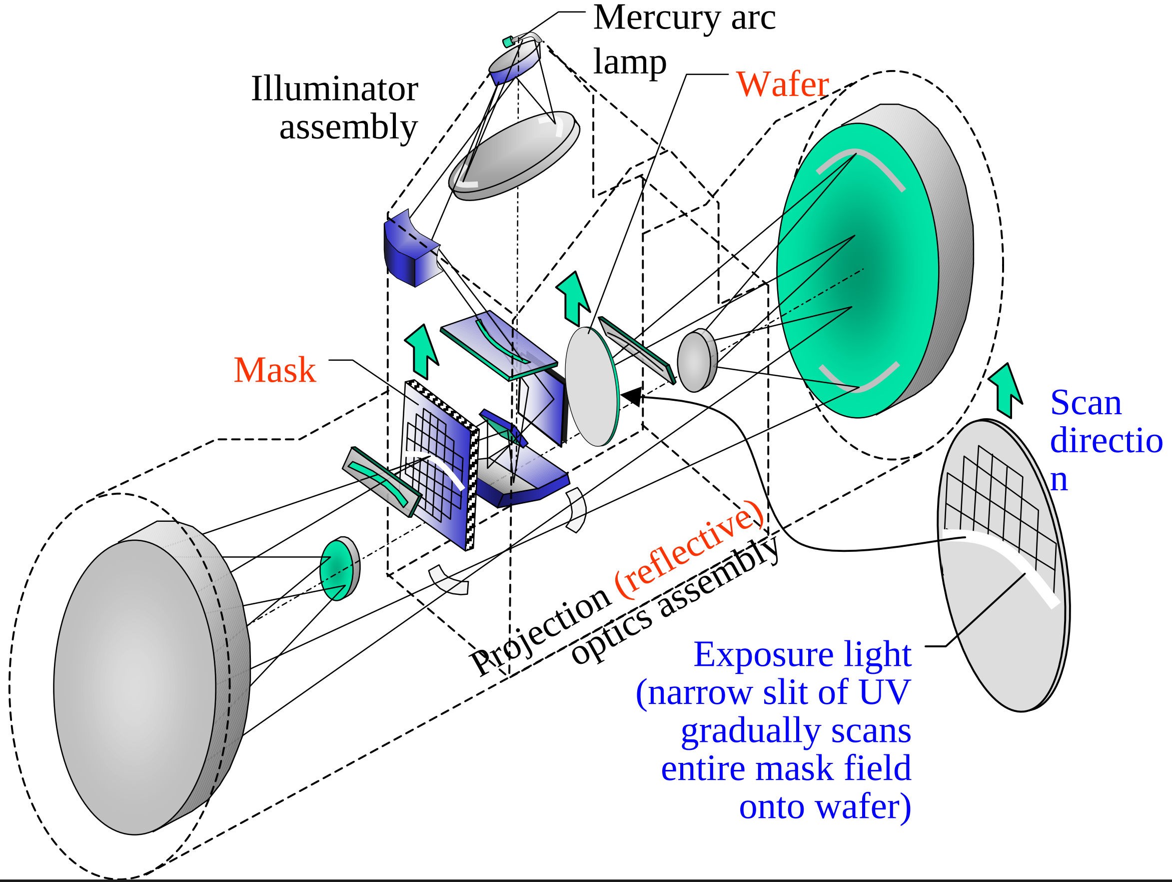


Proximity aligner : gap = 2.5~25 µm

Used with permission from Canon USA,

Photolithography Equipment

(b) Scanning Projection Aligner (Scanner) : 1978~1982



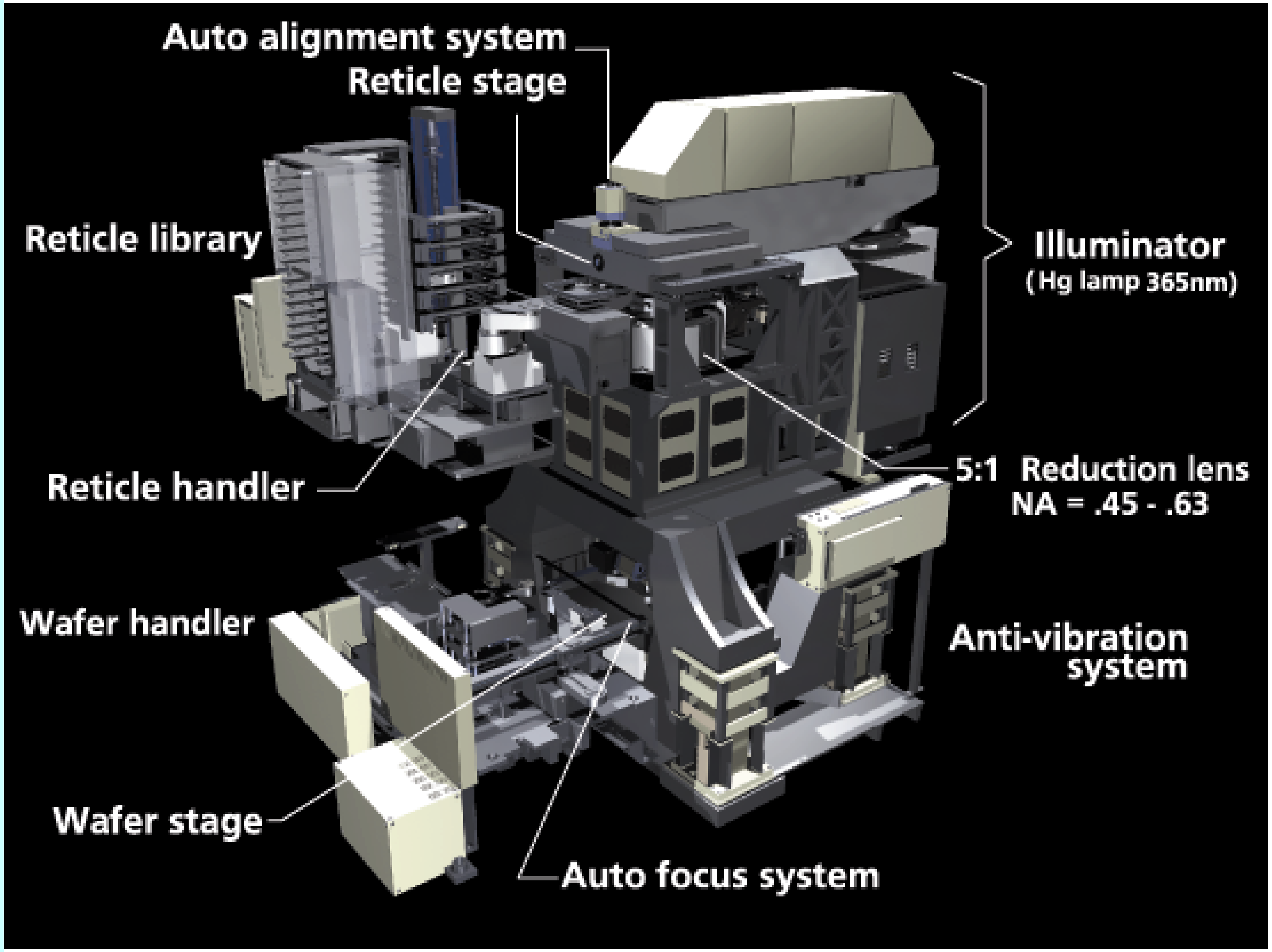
The major challenge of scanner was making a good 1X mask that contained all the chips on the wafer. If the chip had submicron feature sizes, then the mask also had submicron dimensions.

Photolithography Equipment

(c) Step-and-Repeat Aligner (Stepper): 1983~1990s

Steppers have their distinct name because the tool **projects only one exposure field** (which may be one or more chips on the wafer), and then steps to the next location on the wafer to repeat the exposure.

A stepper **use a reticle**, which contains the pattern in an exposure field corresponding to one or more die. A **mask is not used** in a stepper since a mask contains the entire die matrix. The optical projection exposure system of steppers uses **refractive optics** to project the reticle image onto the wafer.



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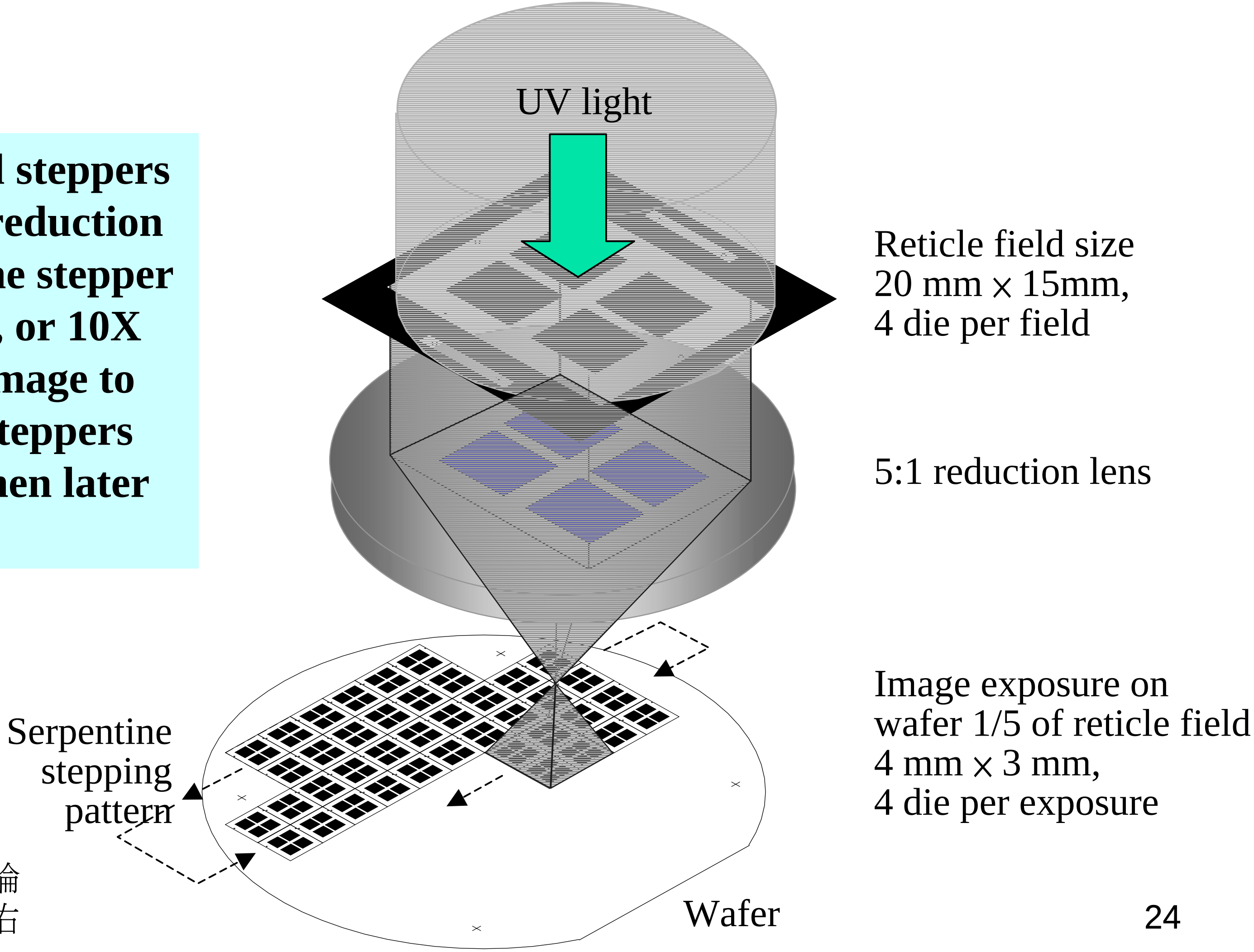
Photolithography Equipment

Stepper Exposure Field

An advantage of optical steppers is their ability to use a reduction lens. Traditionally, I-line stepper reticle are sized 4X, 5X, or 10X larger than the actual image to be patterned (initially steppers used 10X reticles and then later 5X and 4X).

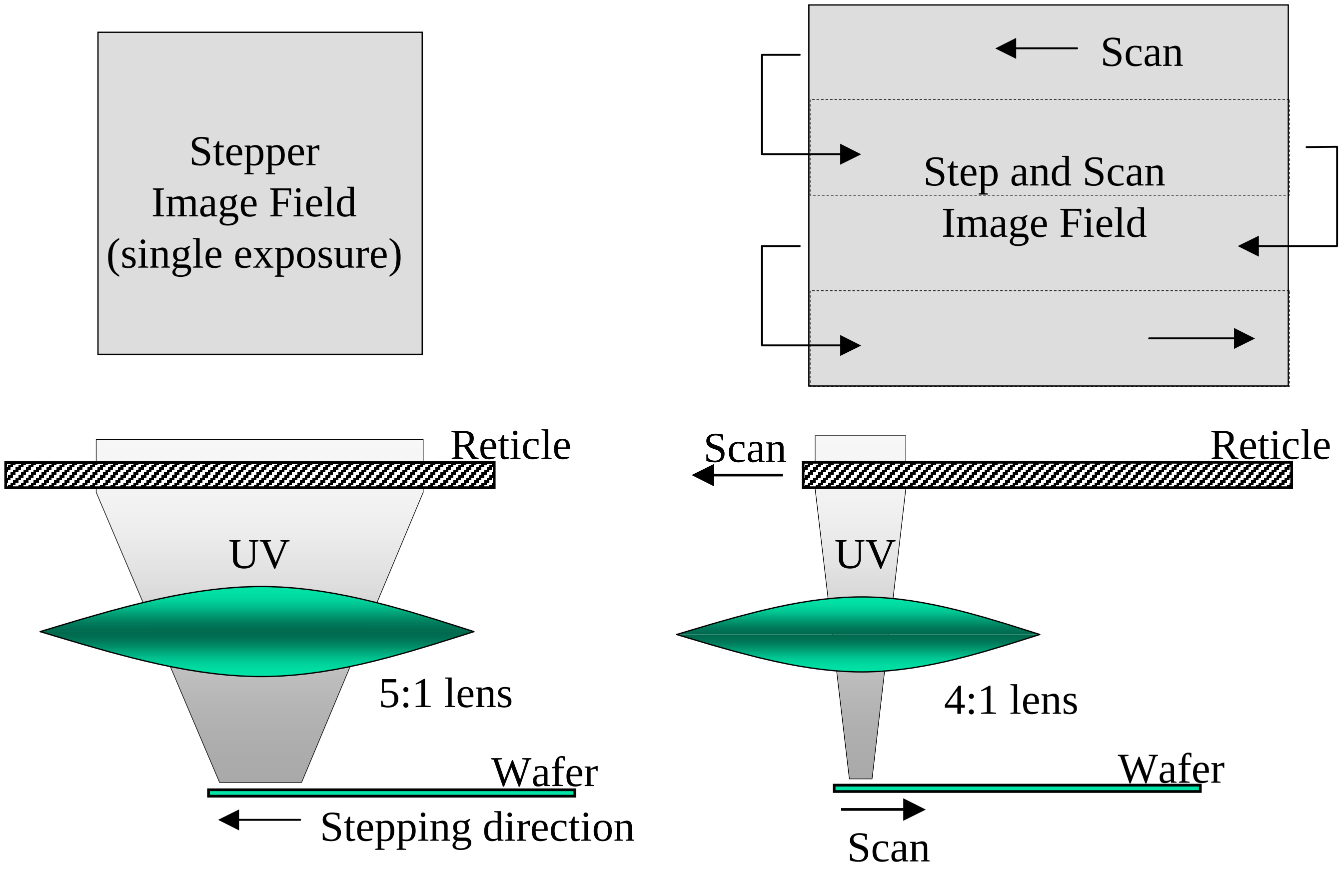


Photolithography Equipment

(d) Step-and-Scan System : 2000s

Benefit:

1. The exposure field is increased for large chip sizes. The lens field only has to be a narrow slit, permitting a smaller lens system.
2. The ability to adjust focus throughout a scan (called on –the-fly focus), permitting compensation for lens defects and changes in wafer flatness. This improved control of focus during a scan yields improved CD uniformity control across the exposure field.

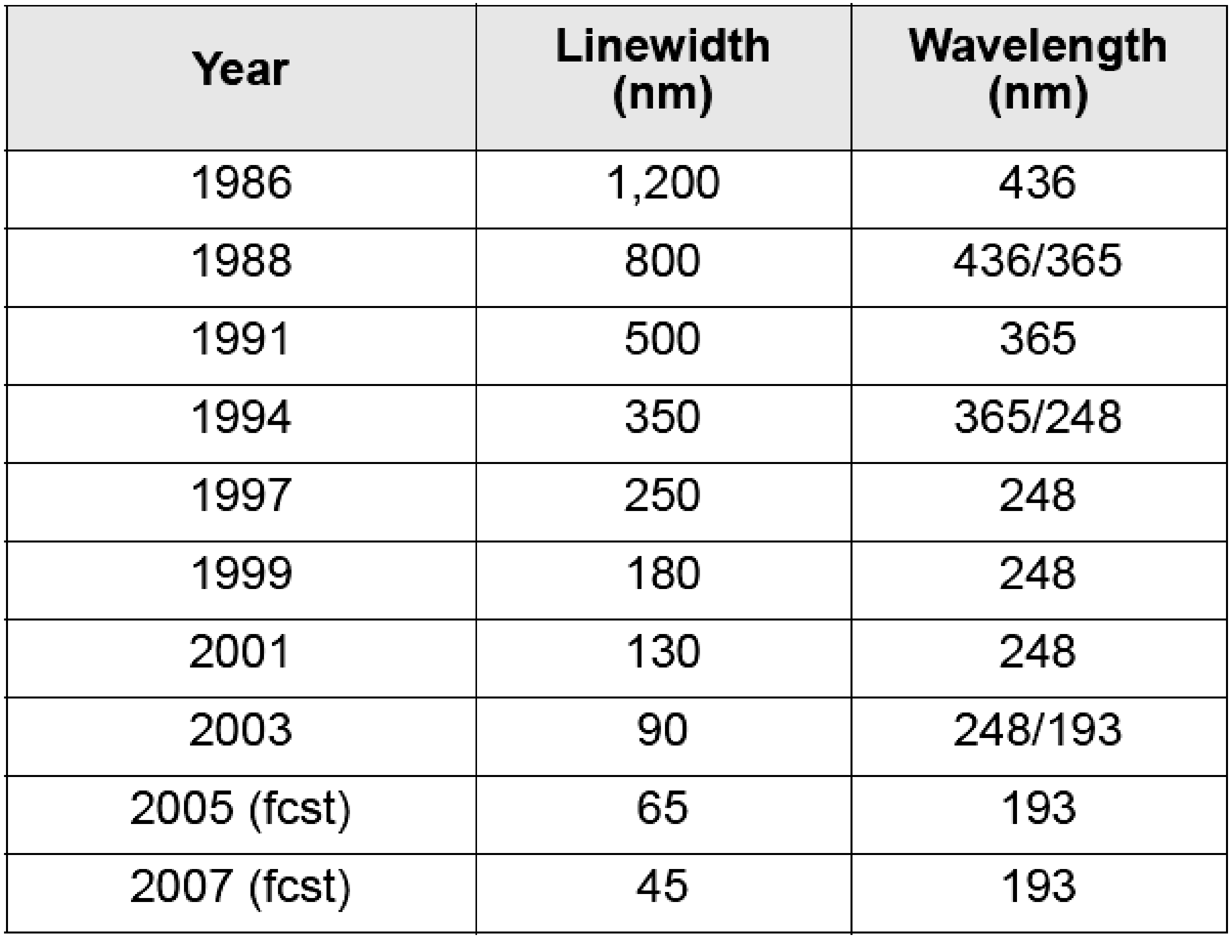


Wafer Exposure Field for Step-and-Scan

Light Sources

- Ultraviolet (UV) light
- Deep ultraviolet (DUV) light
- Ion beam

Minimum linewidth and exposure wavelength



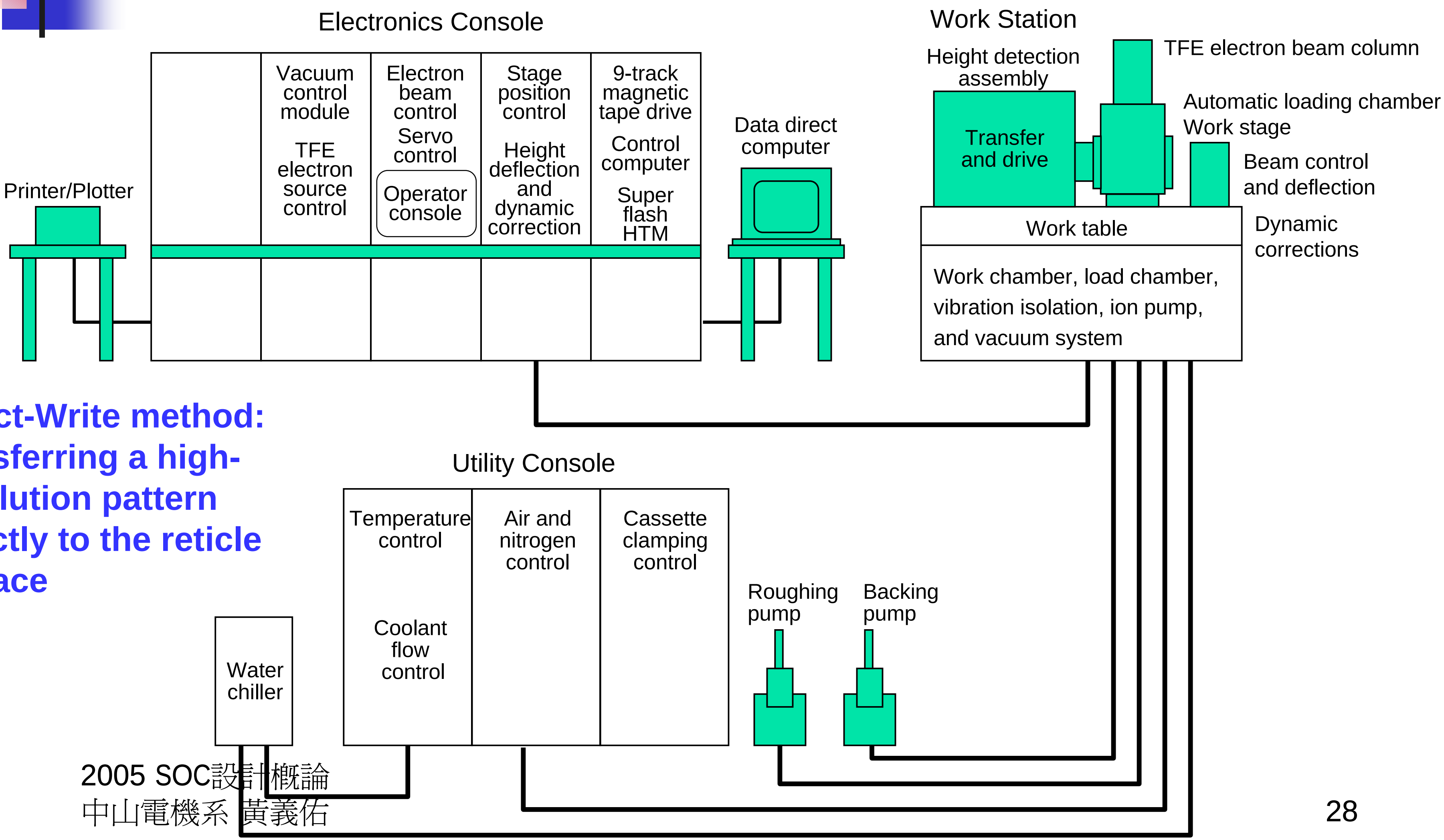
Year	Linewidth (nm)	Wavelength (nm)
1986	1,200	436
1988	800	436/365
1991	500	365
1994	350	365/248
1997	250	248
1999	180	248
2001	130	248
2003	90	248/193
2005 (fcst)	65	193
2007 (fcst)	45	193

Comparison of Reticle Versus Mask

Parameter	Reticle (Pattern for Step-and-Repeat Exposure)	Mask (Pattern for 1:1 Mask-Wafer Transfer)
Critical Dimension	Easier to pattern submicron dimensions on wafer due to larger pattern size on reticle (e.g., 4:1, 5:1).	Difficult to pattern submicron dimensions on mask and wafer without reduction optics.
Exposure Field	Small exposure field that requires step-and-repeat process.	Exposure field is entire wafer.
Mask Technology	Optical reduction permits larger reticle dimensions – easier to print.	Mask has same critical dimensions as wafer – more difficult to print.
Throughput	Requires sophisticated automation to step-and-repeat across wafer.	Potentially higher (not always true if equipment is not automated).
Die alignment & focus	Adjusts for individual die alignment & focus.	Global wafer alignment, but no individual die alignment & focus.
Defect density	Improved yield but no reticle defect permitted. Reticle defects are repeated for each field exposure.	Defects are not repeated multiple times on a wafer.
Surface flatness	Stepper compensates during initial global pre-alignment measurements or during die-by-die exposures.	No compensation, except for overall global focus and alignment.

Principles of Electron Beam Lithography

E-beam mask writer



Electronics Console

Vacuum control module

TFE electron source control

Electron beam control

Servo control

Operator console

Stage position control

Height deflection and dynamic correction

9-track magnetic tape drive

Control computer

Super flash HTM

Printer/Plotter

Data direct computer

Work Station

Height detection assembly

Transfer and drive

TFE electron beam column

Automatic loading chamber

Work stage

Beam control and deflection

Work table

Dynamic corrections

Work chamber, load chamber, vibration isolation, ion pump, and vacuum system

Utility Console

Temperature control

Coolant flow control

Air and nitrogen control

Cassette clamping control

Water chiller

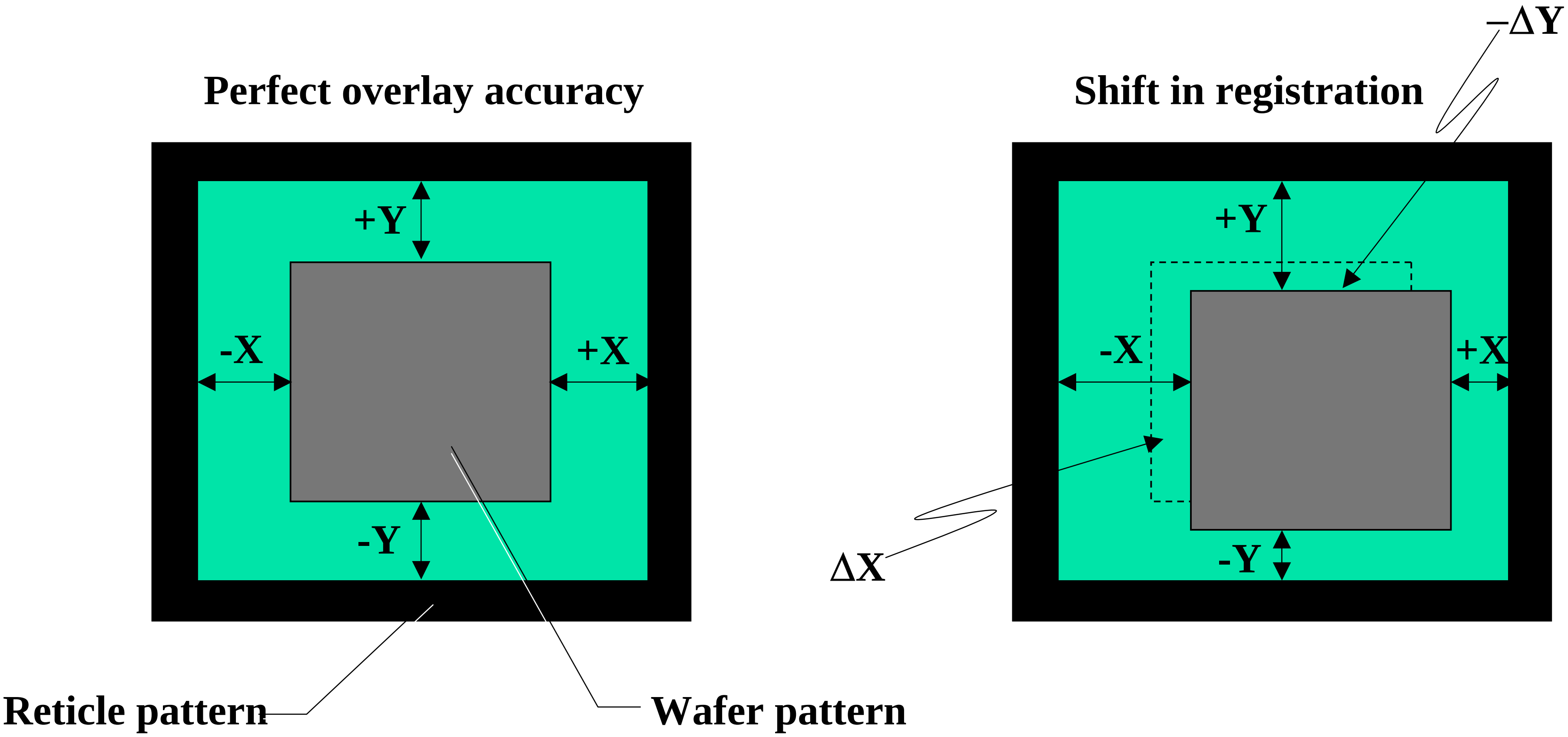
Roughing pump

Backing pump

Direct-Write method: transferring a high-resolution pattern directly to the reticle surface

Alignment

Overlay accuracy is the measure of the alignment system’s ability to overlay the reticle pattern onto the wafer pattern. Overlay budget describes the maximum relative displacement between a patterned layer and the previously defined layer. In general, the overlay budget is about one-third of the critical dimension. For 0.15µm design rules, the overlay budget is expected to be 50nm.

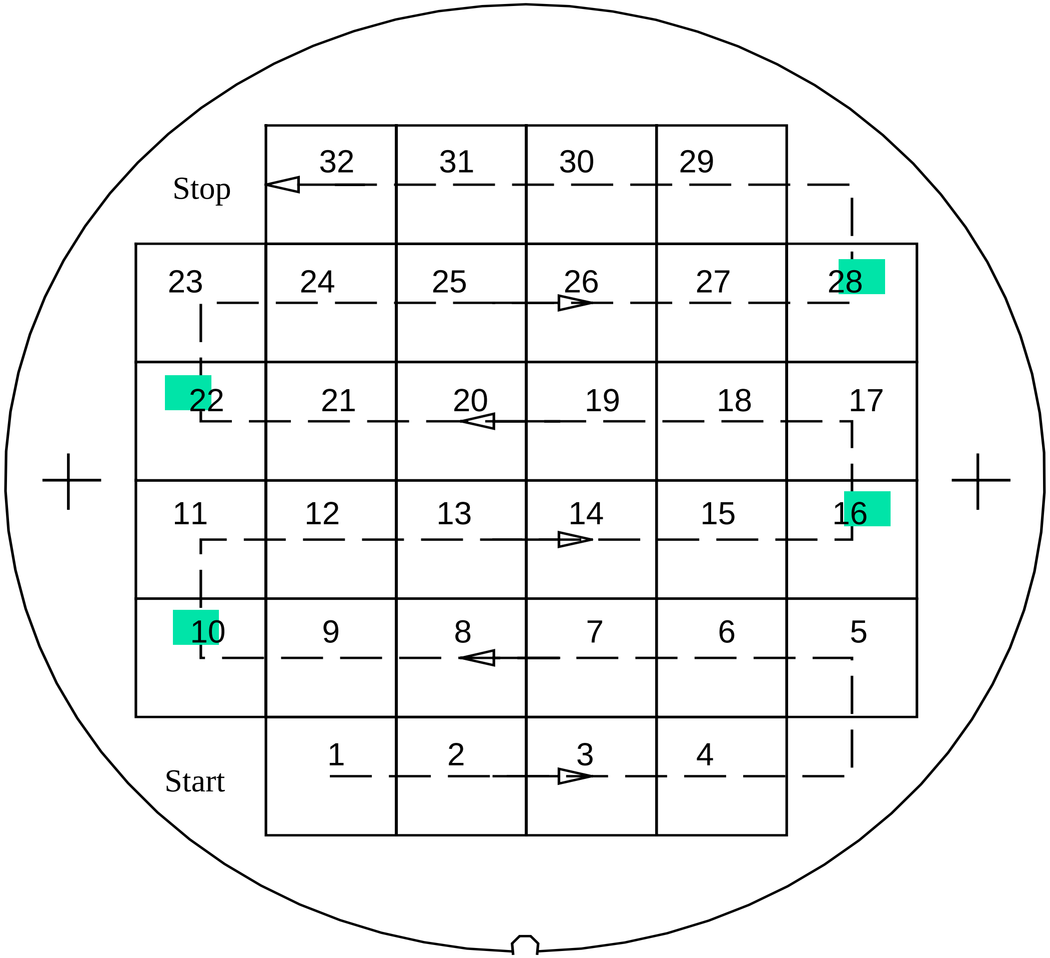


Overlay Budget

Alignment

For steppers and step-and-scan systems, each reticle pattern is aligned and exposed at multiple locations as the aligner steps across the wafer. Each field corresponds to the reticle pattern of a single large chip or several smaller chips.

A *grid* is the particular path that the photo tool follows to step across the wafer and expose the individual fields.



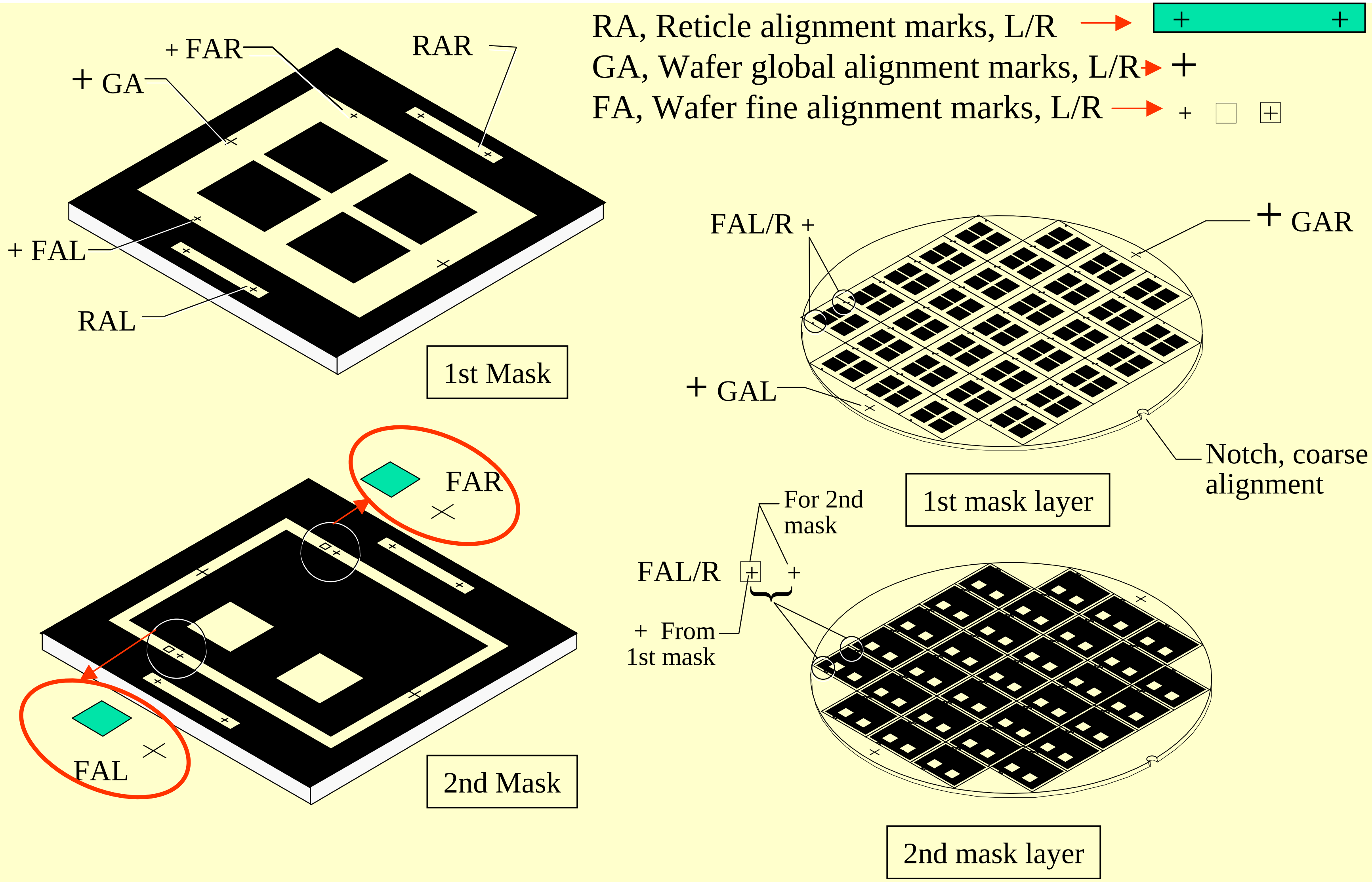
Grid of Exposure Fields on Wafer

Alignment Marks

RA, Reticle alignment marks, L/R → + +

GA, Wafer global alignment marks, L/R → +

FA, Wafer fine alignment marks, L/R → + □ ⊞



5. Post-Exposure Bake (PEB) & 6. Photoresist Development

- **PEB is necessary for chemically amplified DUV resists to catalyze critical resist chemical reactions.**
- **PEB is also required for conventional i-line resists (reduce standing wave effect & improve adhesion)**
- **Typical PEB Temperatures 100 to 110°C on a hot plate**
- **PEB process is immediately after Exposure process.**

Development Process Summary:

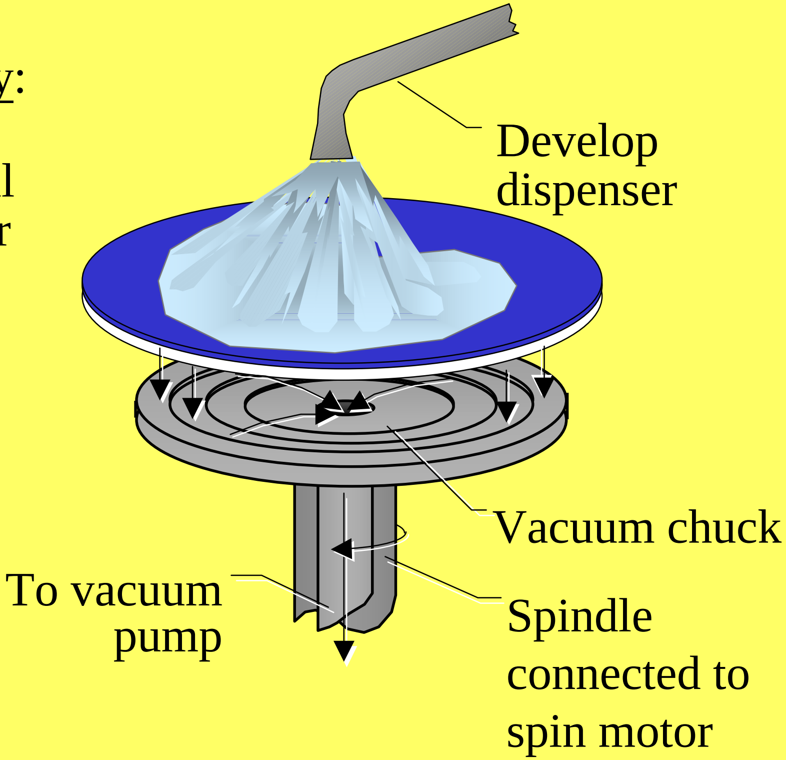
Soluble areas of photoresist are dissolved by developer chemical

Visible patterns appear on wafer

- windows
- islands

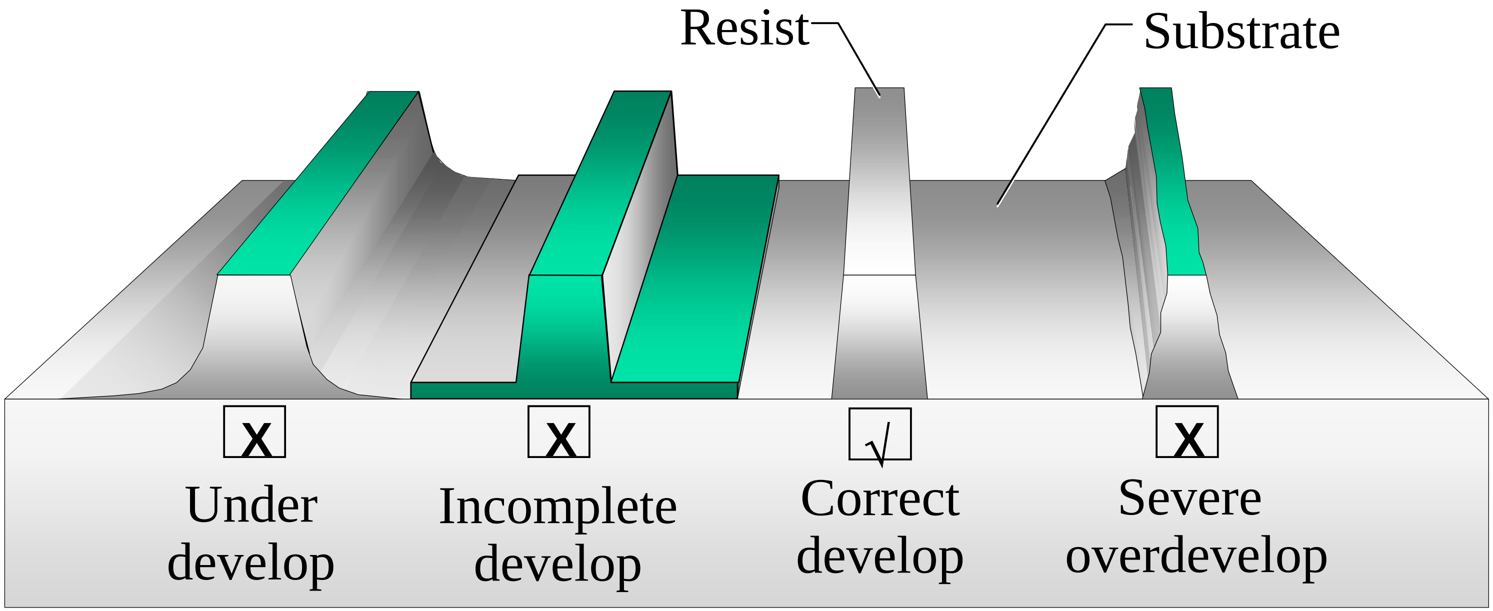
Quality measures:

- line resolution
- uniformity
- particles and defects

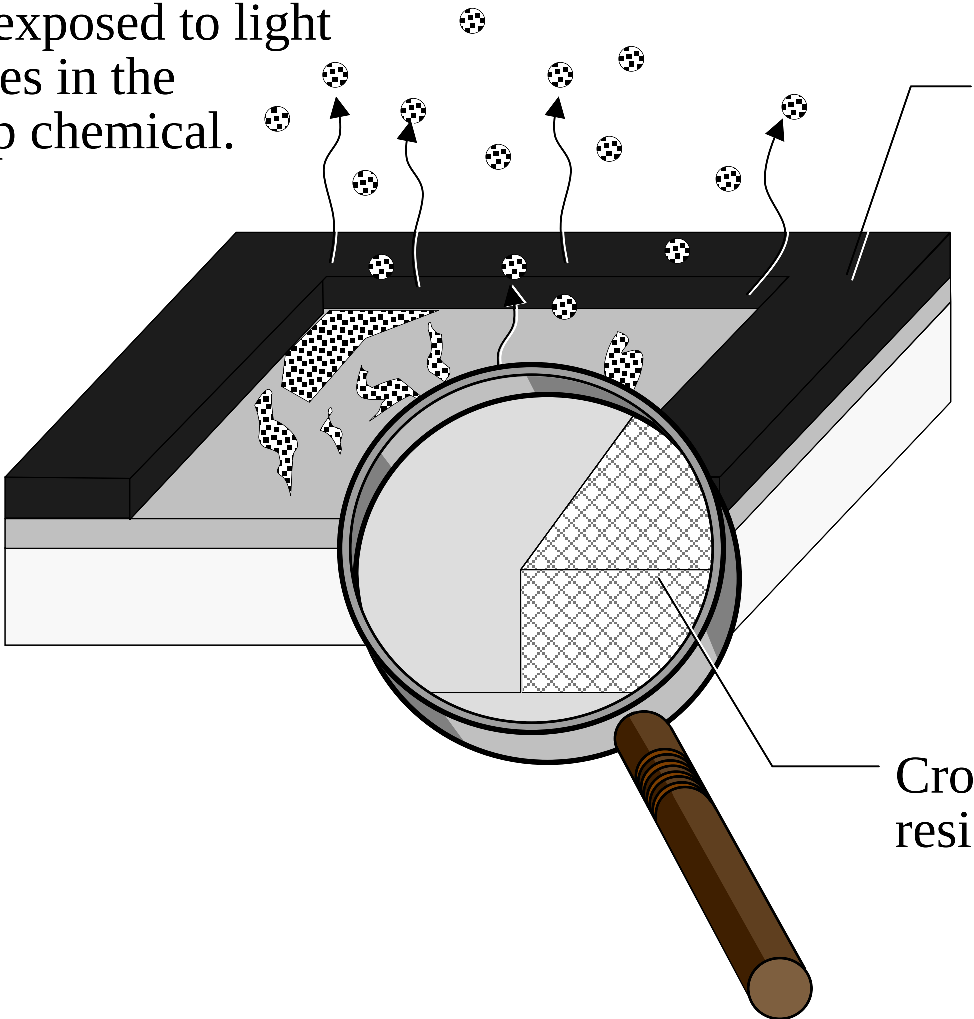


Develop

Photoresist Development Problems



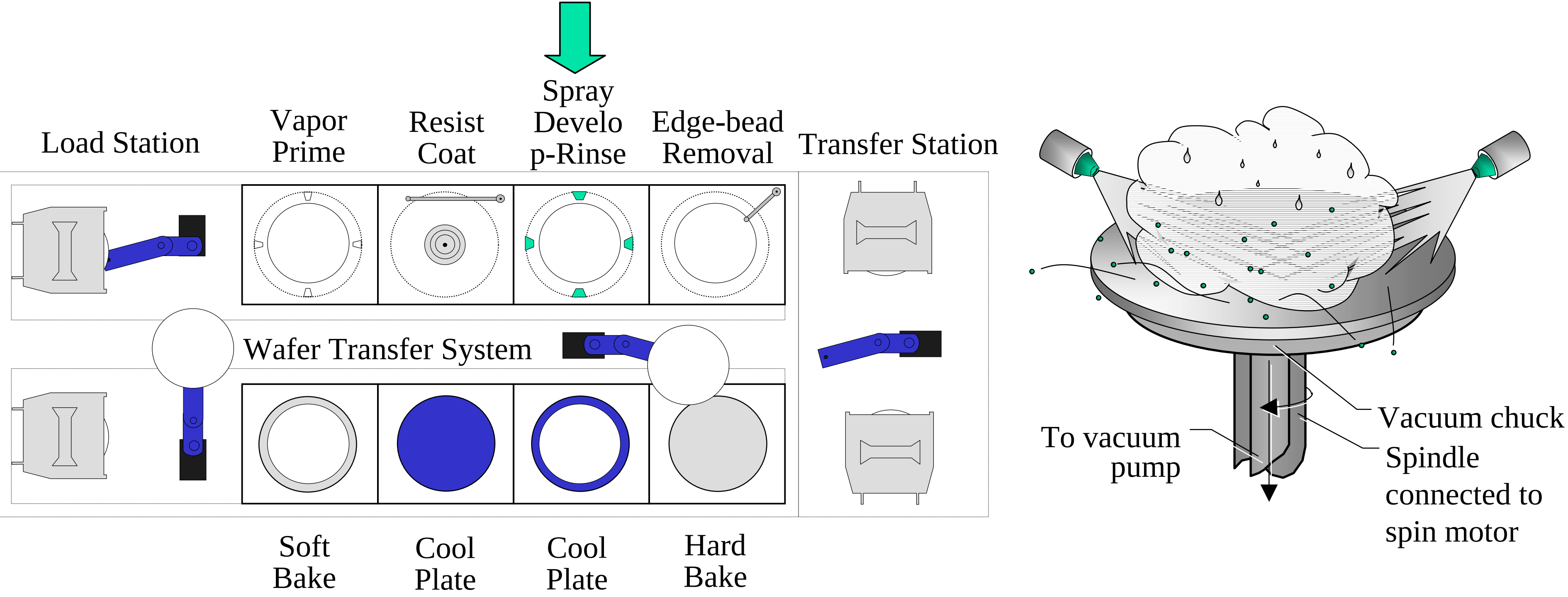
Development of Positive Resist



Resist Development Parameters

- **Developer Temperature**
- **Developer Time**
- **Developer Volume**
- **Normality**
- **Rinse**
- **Exhaust Flow**
- **Wafer Chuck**

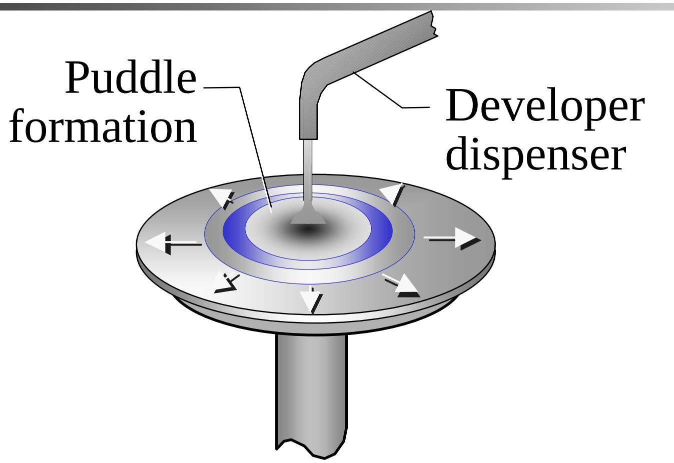
Resist Development with Continuous Spray



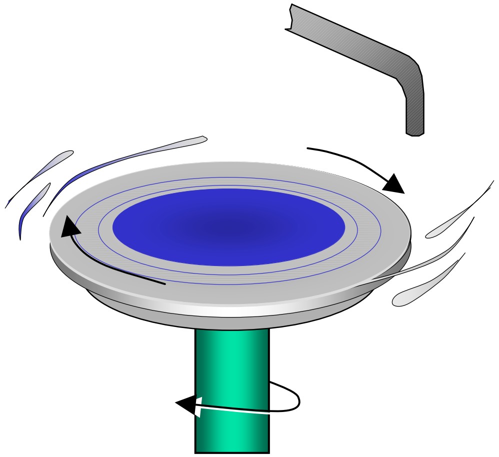
(a) Wafer track system

(b) Developer spray dispenser

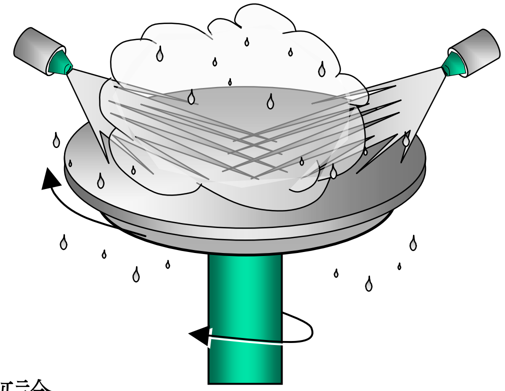
Puddle Resist Development



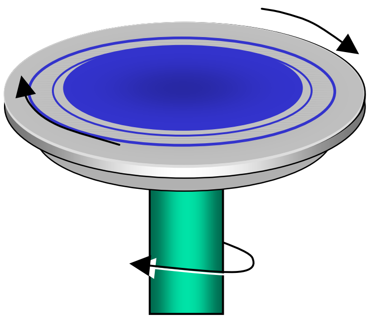
(a) Puddle dispense



(b) Spin-off excess developer



(c) DI H_2O rinse

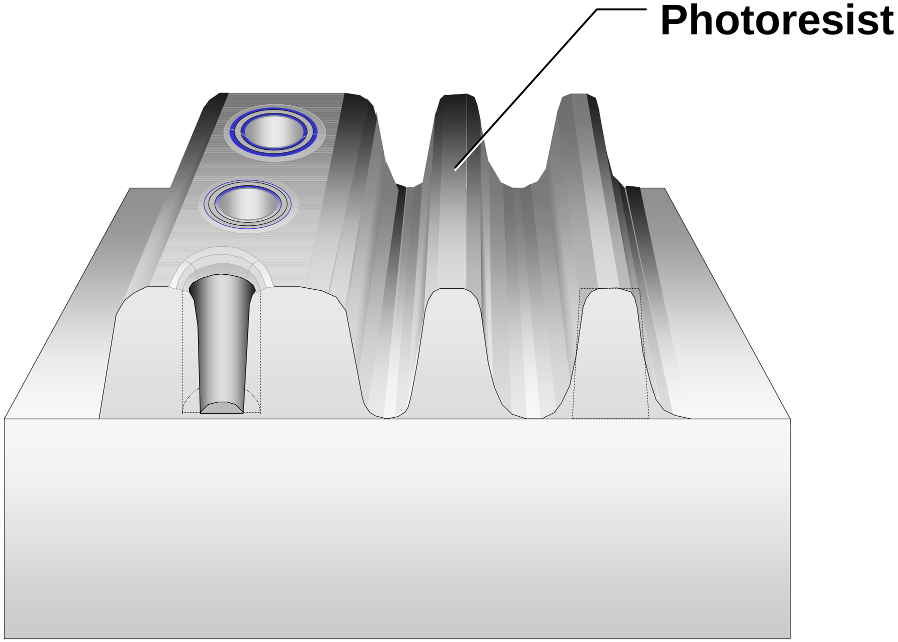


(d) Spin dry

7. Hard Bake

- A Post-Development Thermal Bake
- Evaporate Remaining Solvent
- Improve Resist-to-Wafer Adhesion
- Higher Temperature (120 to 140°C) than Soft Bake

- Characteristics of Hard Bake:
  - Post-Development Exposure
  - Evaporates Residual Solvent in Photoresist
  - Hardens the Resist
  - Improves Resist-to-Wafer Adhesion
  - Prepares Resist for Subsequent Processing
  - Higher Temperature than Soft Bake, but not to Point Where Resist Softens and Flows
- Resist Hardening with Deep UV



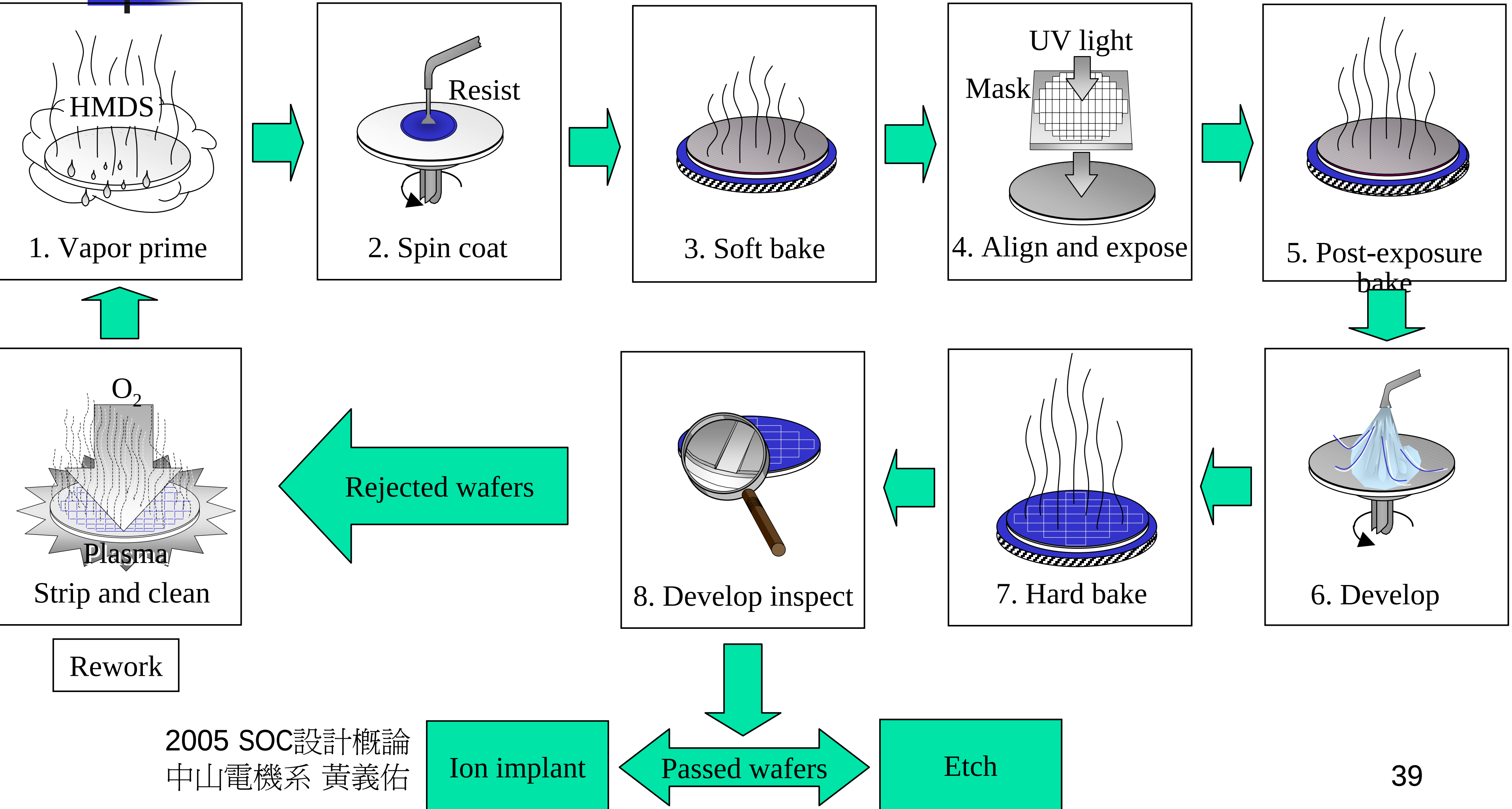
Softened Resist Flow at High Temperature

8. Develop Inspect

- Post-Develop Inspection to Find Defects
- Find Defects before Etching or Implanting
- Prevents Scrap
- Characterizes the Photo Process by Providing Feedback Regarding Quality of the Lithography Process
- Develop Inspect Rework Flow
- Typically an Automated Operation

Automated Inspection Tool for Develop Inspect

Develop Inspect Rework Flow



1. Vapor prime
2. Spin coat
3. Soft bake
4. Align and expose
5. Post-exposure bake
6. Develop
7. Hard bake
8. Develop inspect

Rejected wafers

Strip and clean

Rework

Passed wafers

Ion implant

Etch