Outline

1. **Introduction to the Semiconductor Industry (3 hrs)**
2. **Semiconductor Materials & Devices (3 hrs)**
3. **ULSI Manufacturing Technology (12 hrs)**

   (a) Oxidation/Diffusion (b) Thin Film Deposition & Metallization

   (c) Photolithography (d) Etch (e) Chemical Mechanical Planarization
4. **ULSI Process Integration (0.18 μm CMOS Process) (3 hrs)**
5. **IC Design Rules (3 hrs)**

1. **Semiconductor Manufacturing Technology**
   : Michael Quirk and Julian Serda (2001)

2. 國家矽導計畫-教育部晶片法商學程教材 **(2004)**

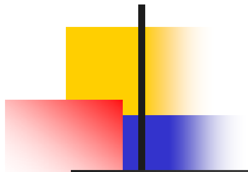
3. **Semiconductor Physics and Devices- Basic Principles(3/e)**
   : Donald A. Neamen (2003)

4. **Semiconductor Devices - Physics and Technology (2/e)**
   : S. M. Sze (2002)

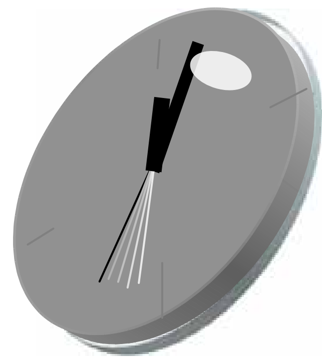
5. **ULSI Technology** ***: C. Y. Chang, S. M. Sze (1996)***

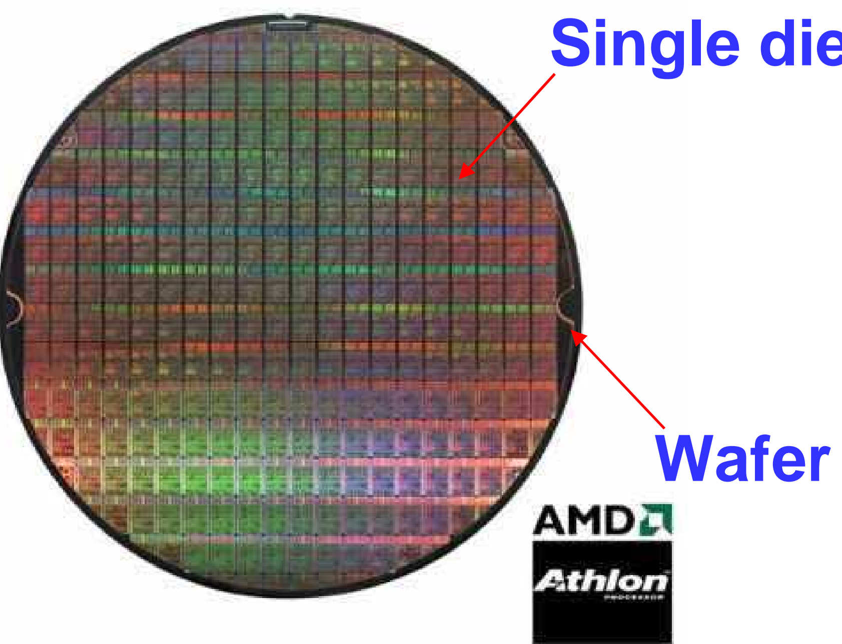
課程相關資訊

- 修課人數：125 人 (工: 106 / 管：13 / 理：3 / 文：1 / 社科: 2)
- 上課時間：18:20 ~ 21:10
- 上課地點：F1001教室
- 教材分享：中山課程網 (http://www.course.nsysu.edu.tw)
- 助教名單：蔡漢城, 李新仁, 陳晟瑋, 佘坤典 (分機：4128)
- 課後指導：14:00 ~ 17:00 (一) ; F6002黃義佑老師辦公室
- 成績評量：平時成績(20%) ; 期中考(40%) ; 期末考(40%)



Time to Market





Design

Fabrication

order

Package

Testing

From http://www.amd.com

Photo courtesy of
Advanced Micro Devices

The Semiconductor Industry

Worldwide sales of microchips : > $200 billion in 2002

SIA: semiconductor industry association

Photo courtesy of Advanced Micro Devices-Dresden, © S. Doering

Wafer Fab

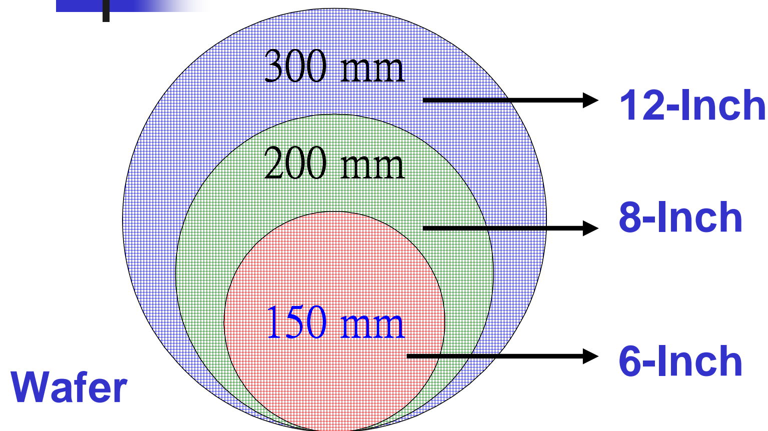
Circuit Integration of Semiconductors - Integration Eras

Circuit Integration	Semiconductor Industry Time Period	Number of Components per Chip
No integration (discrete components)	Prior to 1960	1
Small scale integration (SSI)	Early 1960s	2 to 50
Medium scale integration (MSI)	1960s to Early 1970s	50 to 5,000
Large scale integration (LSI)	Early 1970s to Late 1970s	5,000 to 100,000
Very large scale integration (VLSI)	Late 1970s to Late 1980s	100,000 to 1,000,000
Ultra large scale integration (ULSI)	1990s to present	> 1,000,000

Semiconductor Trends :

- Increase in Chip Performance
  - Components per Chip ↑ & Power Consumption ↓
- Increase in Chip Reliability
- Reduction in Chip Price

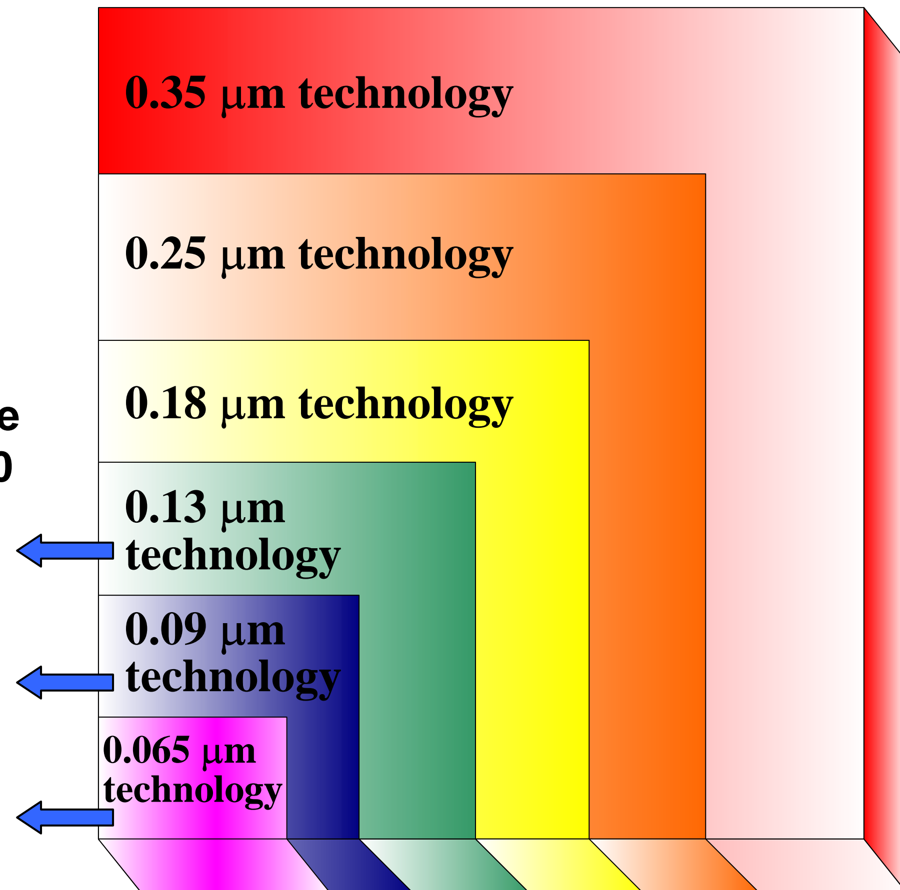
Feature Technology and Size



When compared to the 0.18-micron process, the new 0.13-micron process results in less than 60 percent the die size and nearly 70 percent improvement in performance

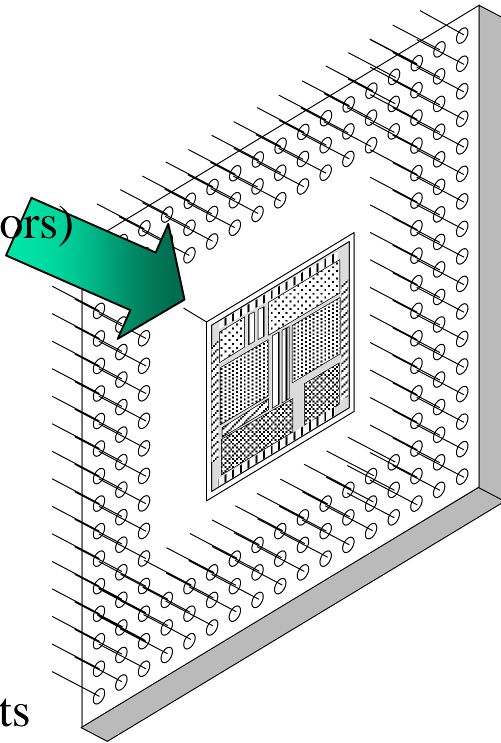
The 90-nm process will be manufactured on 300mm wafers

NEC devises low-k film for second-generation 65-nm process



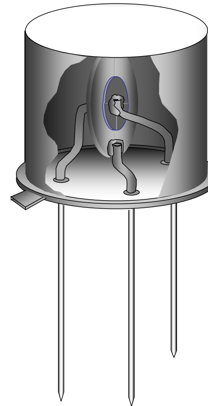
ULSI Chip

1990s Microchip
(5~25 million transistors)



U.S. coin, 10 cents

1960s Transistor



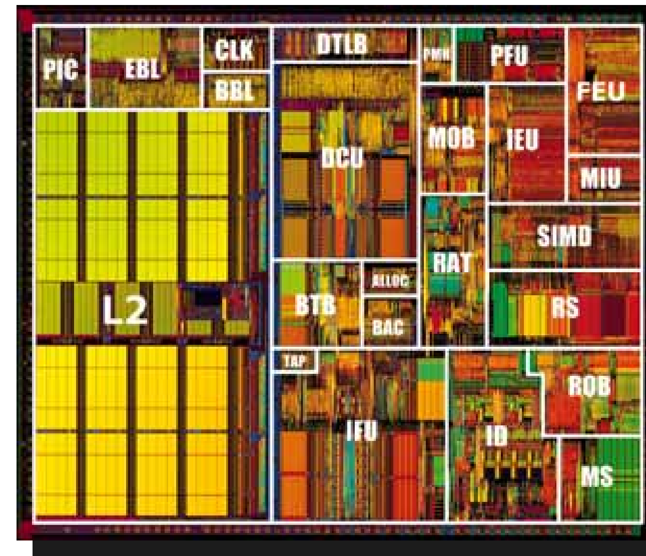
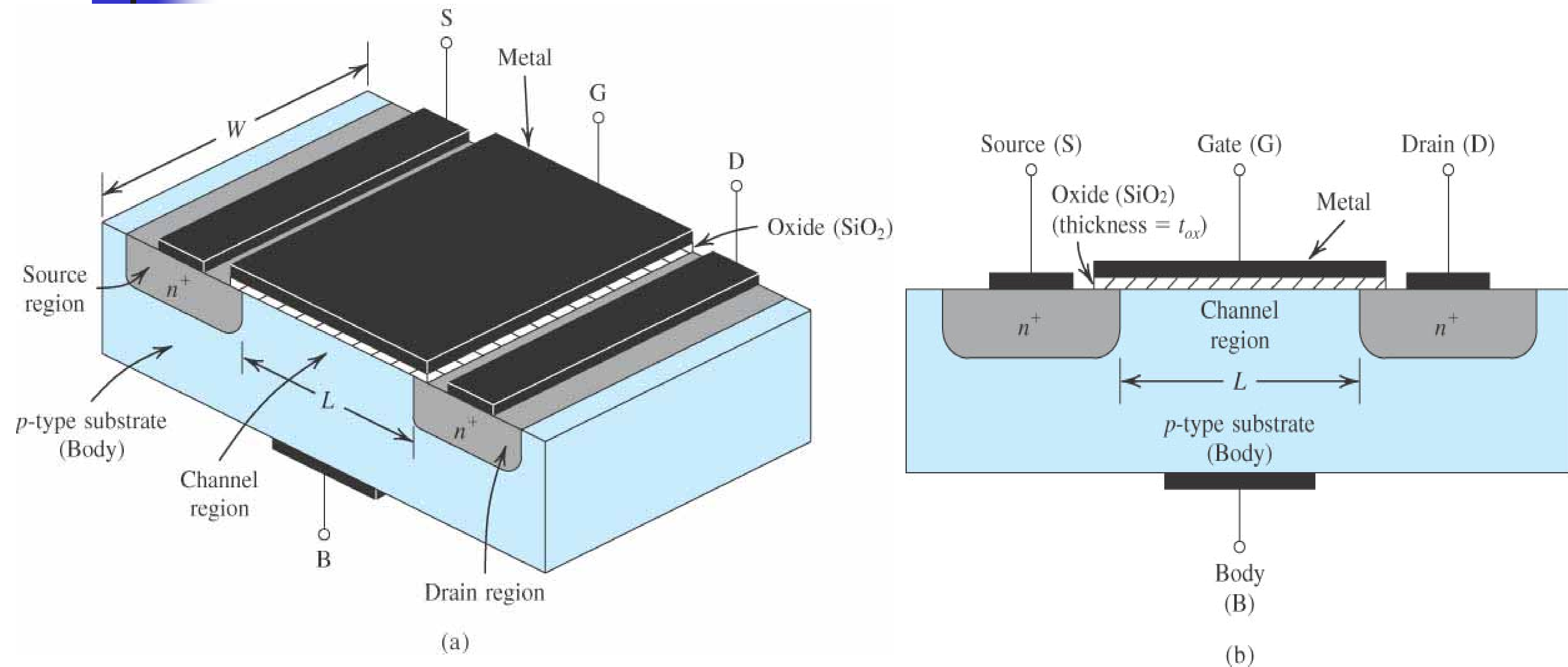


Photo courtesy of Intel Corporation, Pentium III

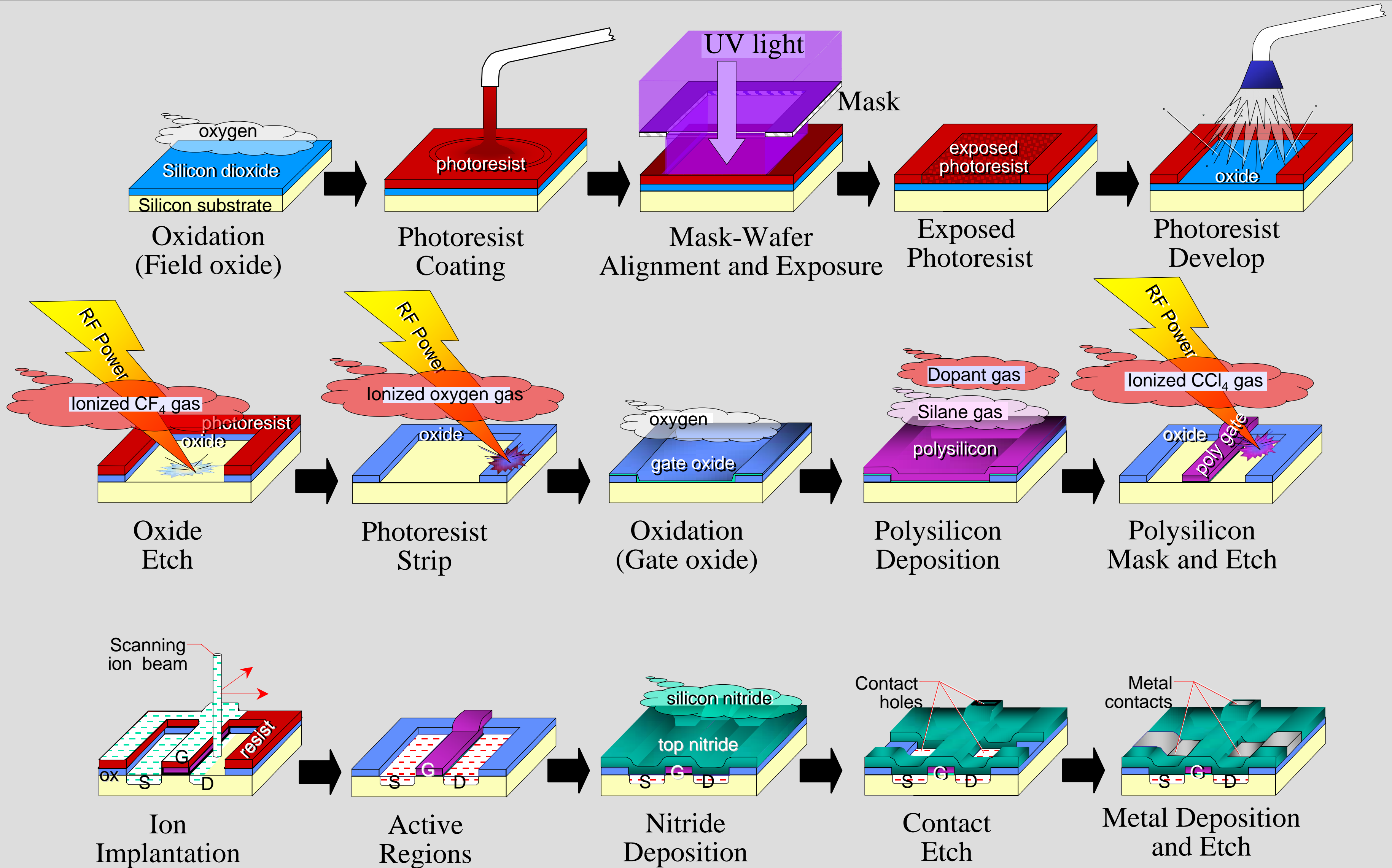
Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)



Physical structure of the enhancement-type NMOS transistor: (a) perspective view; (b) cross-section. Typically L = 0.1 to 3 mm, W = 0.2 to 100 mm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

IC Fabrication Process Overview

Major Fabrication Steps in MOS Process Flow



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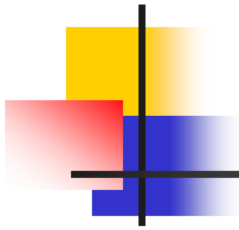
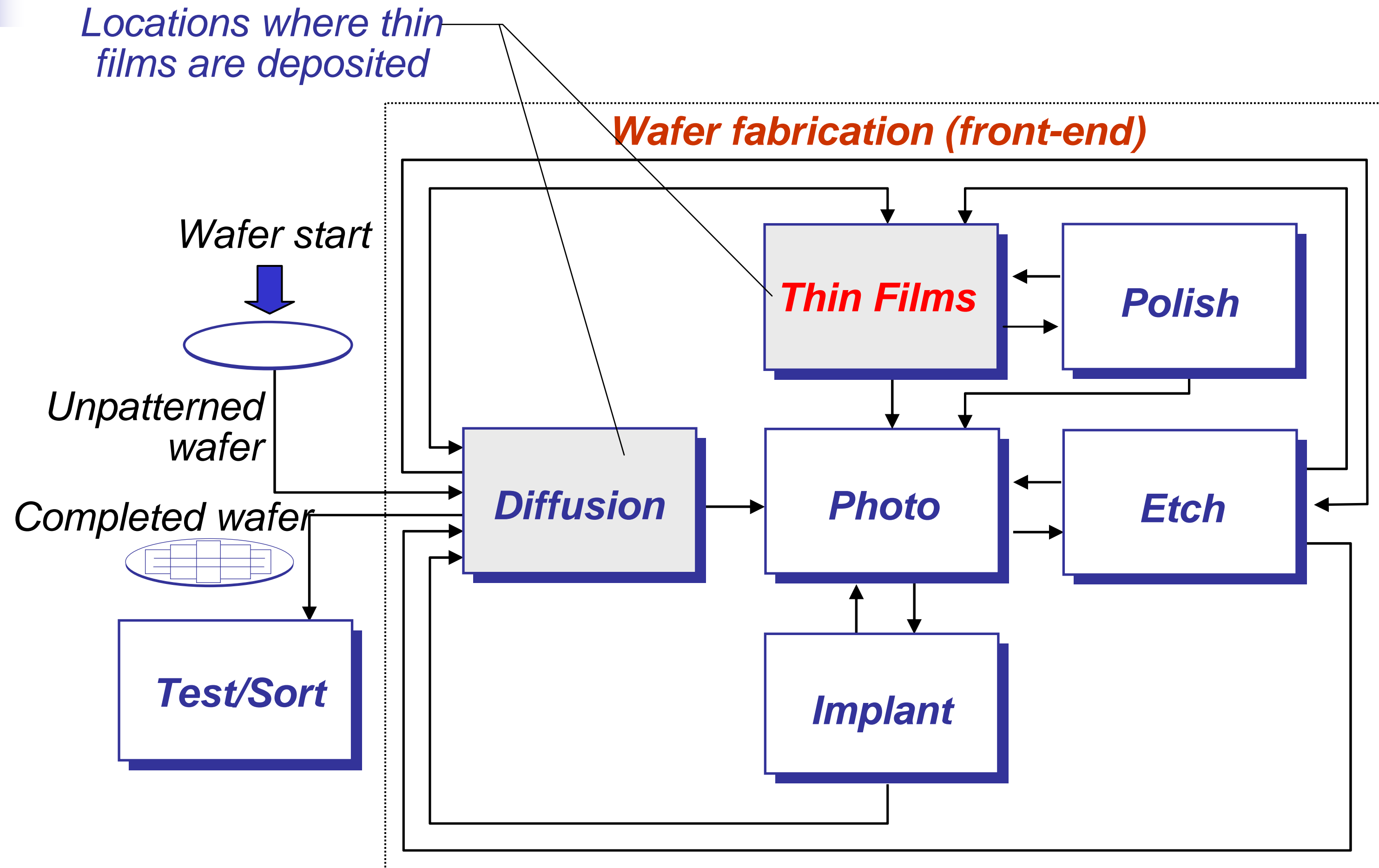


Chapter 3 : ULSI Manufacturing Technology
- (b) Thin Film Deposition & Metallization

Process Flow in a Wafer Fab



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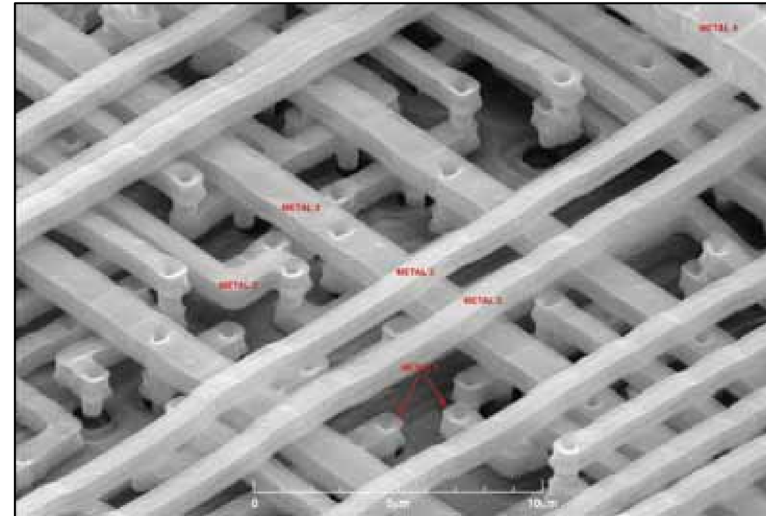
Multilevel Metallization on a ULSI Wafer

Passivation layer
Bonding pad metal
ILD-6
ILD-5
M-4
ILD-4
M-3
ILD-3
M-2
ILD-2
M-1
Via
ILD-1
Poly gate
LI metal
LI oxide
n^+
p^+
p^+
STI
n^+
n^+
p^+
n-well
p-well
p^- Epitaxial layer
p^+ Silicon substrate

Thin Film Deposition

Metal Layers in a Chip



Micrograph courtesy of Integrated Circuit Engineering

Techniques of Film Deposition

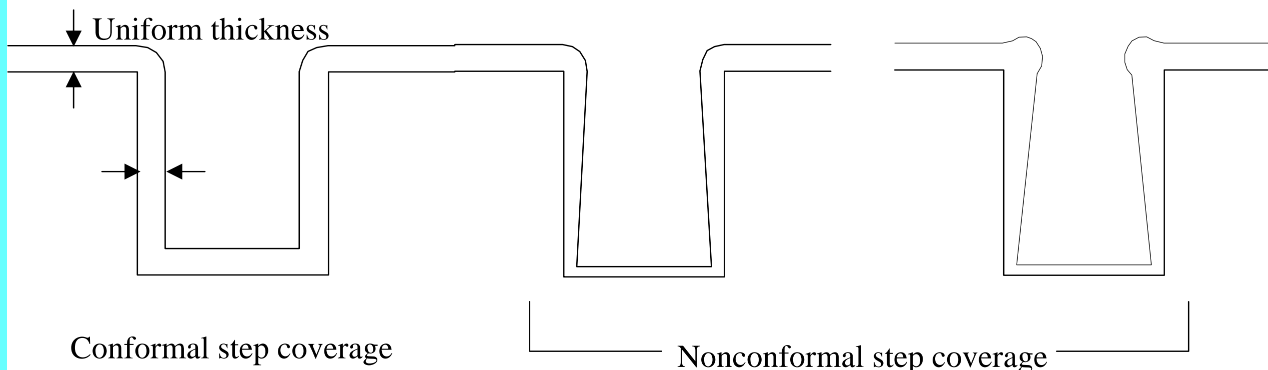
Chemical Processes		Physical Processes		
Chemical Vapor Deposition (CVD)	**Plating**	**Physical Vapor Deposition (PVD or Sputtering)**	**Evaporation**	**Spin On Methods**
Atmospheric Pressure CVD (APCVD) or Sub-Atmospheric CVD (SACVD)	Electrochemical deposition (ECD), commonly referred to as electroplating	DC Diode	Filament and Electron Beam	Spin on glass (SOG)
Low Pressure CVD (LPCVD)	Electroless Plating	Radio Frequency (RF)	Molecular Beam Epitaxy (MBE)	Spin on dielectric (SOD)
Plasma Assisted CVD: ▪ Plasma Enhanced CVD (PECVD) ▪ High Density Plasma CVD (HDPCVD)		DC Magnetron		
Vapor Phase Epitaxy (VPE) and Metal-organic CVD (MOCVD)		Ionized metal plasma (IMP)		

1. **Chemical Vapor Deposition (CVD):**
   - APCVD (Atmospheric CVD)
   - LPCVD (Low Pressure CVD)
   - PECVD (Plasma Enhanced CVD)
   - Photon Induced CVD (PHCVD)
   - Metal CVD (Electroplating)
2. **Physical Vapor Deposition (PVD):**
   - Evaporation
   - Sputtering
3. **Epitaxial Growth:**
   - LPE (Liquid-Phase Epitaxy)
   - VPE (Vapor-Phase Epitaxy)
   - MBE (Molecular Beam Epitaxy)

Thin Film Deposition

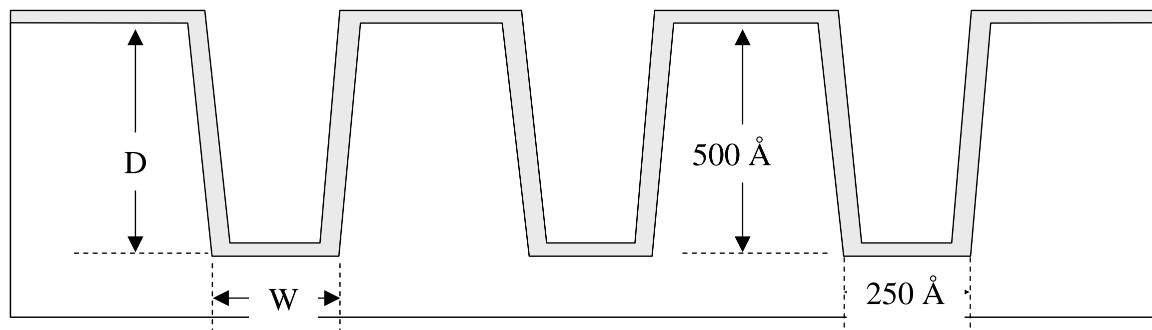
Thin Film Characteristics

- **Good step coverage**
- **Ability to fill high aspect ratio gaps (conformality)**
- **Good thickness uniformity**
- **High purity and density**
- **Controlled stoichiometries**
- **High degree of structural perfection with low film stress**
- **Good electrical properties**
- **Excellent adhesion to the substrate material and subsequent films**



Film Coverage over Steps

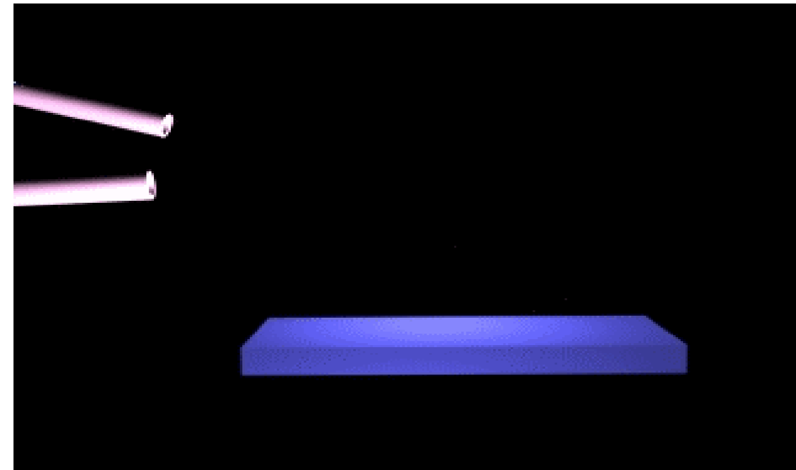
$$\text{Aspect Ratio} = \frac{\text{Depth}}{\text{Width}} \qquad \text{Aspect Ratio} = \frac{500\ \text{Å}}{250\ \text{Å}} = \frac{2}{1}$$



Aspect Ratio for Film Deposition

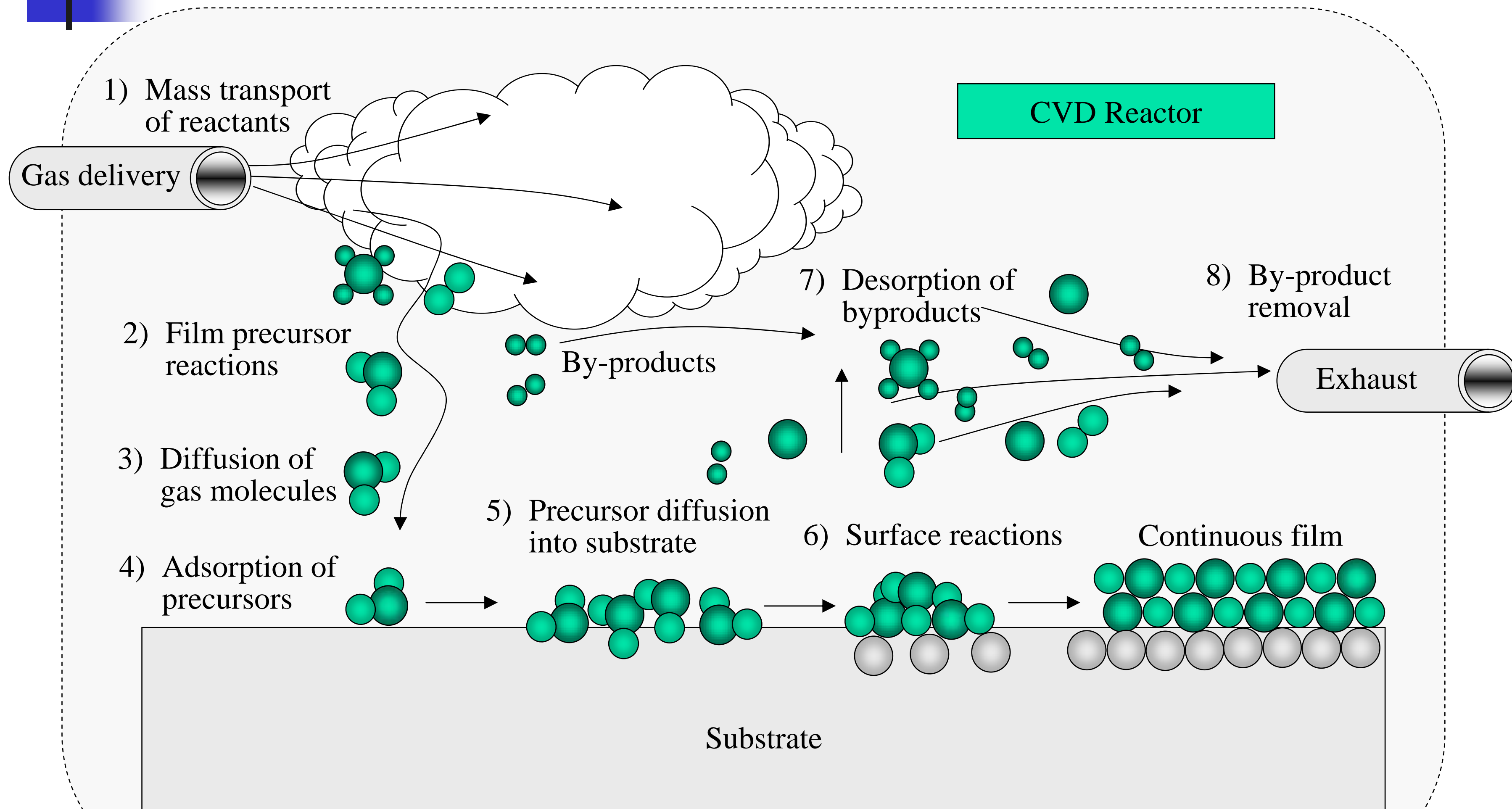
Chemical Vapor Deposition

- A process of depositing films by reacting chemical vapors to produce a film on a substrate
  - May be activated by
    - Heat
    - RF energy (plasma enhanced, PECVD)
    - Light (photon induced, PHCVD)
  - CVD process is used to deposit
    - Poly and single crystal silicon
    - Dielectric films
    - Metal films



Mechanism of Chemical Vapor Deposition (CVD)

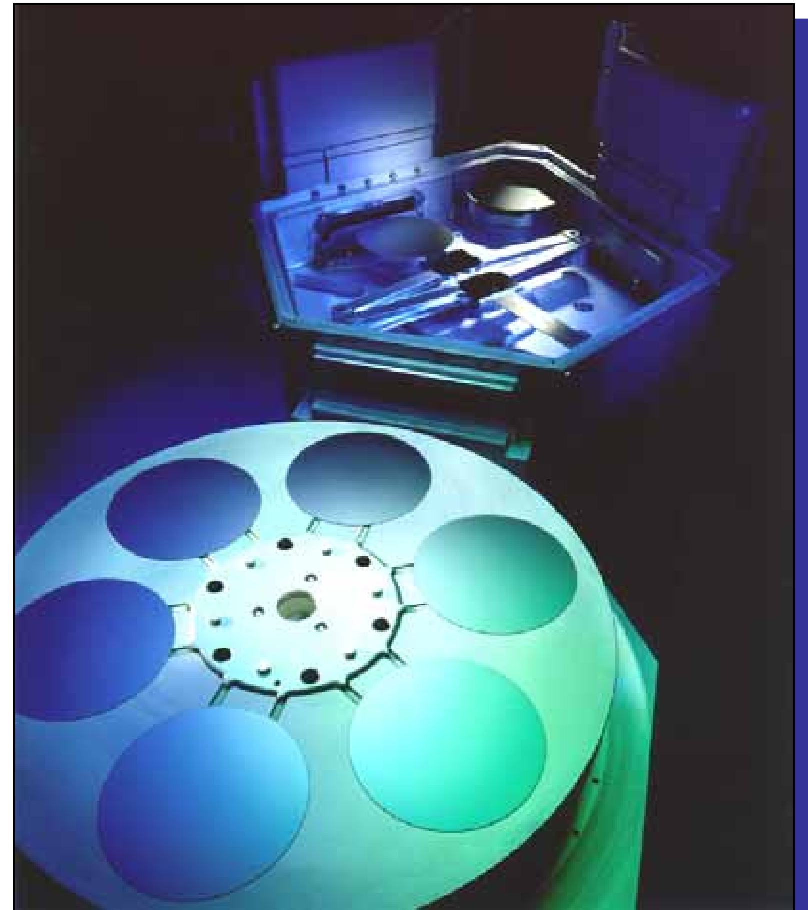
Schematic of CVD Transport and Reaction Steps



CVD Deposition Systems

- **Atmospheric Pressure CVD, APCVD**
- **Low Pressure CVD, LPCVD**
- **Plasma-Assisted CVD**
  1. **Plasma-Enhanced CVD, PECVD**
  2. **High-Density Plasma CVD, HDPCVD**

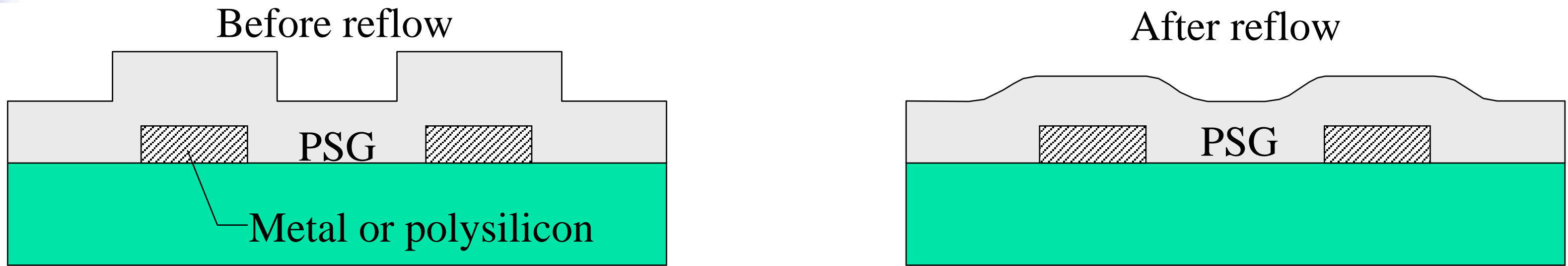
Chemical Vapor Deposition Tool



Photograph courtesy of Novellus, Sequel CVD

Atmospheric Pressure CVD (APCVD) - Applications

Planarized Surface after Reflow of PSG



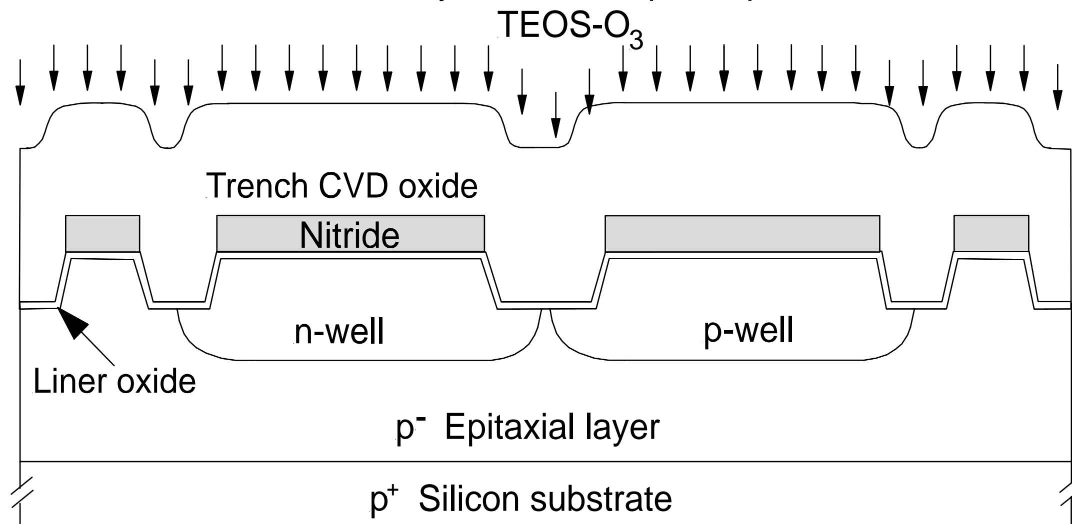
PSG: phosphorusilicate glass

Improved Step Coverage of APCVD 1:8 TEOS-O_3

TEOS: $Si(C_2H_5O)_4$

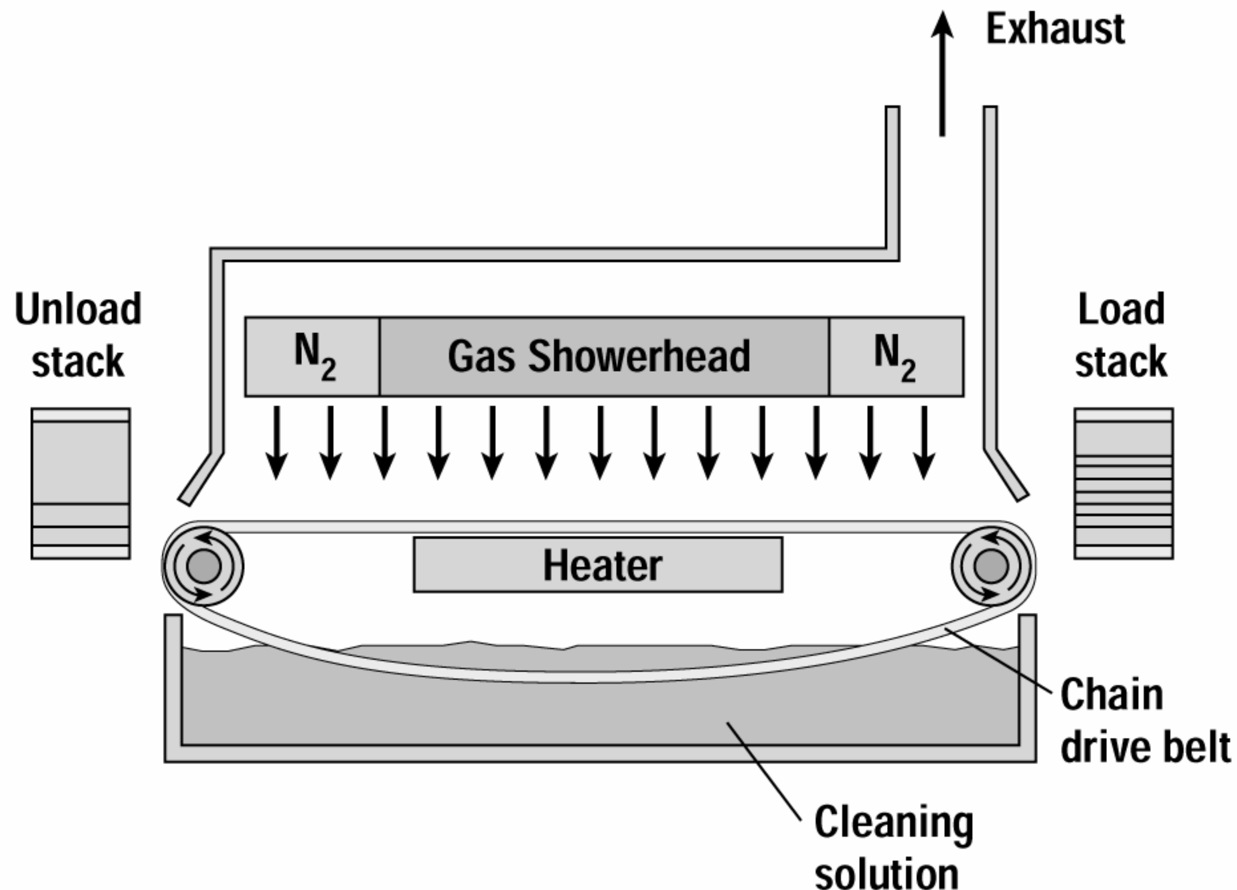
Tetra-ethyl-ortho-silicate

（四乙基正矽酸鹽）



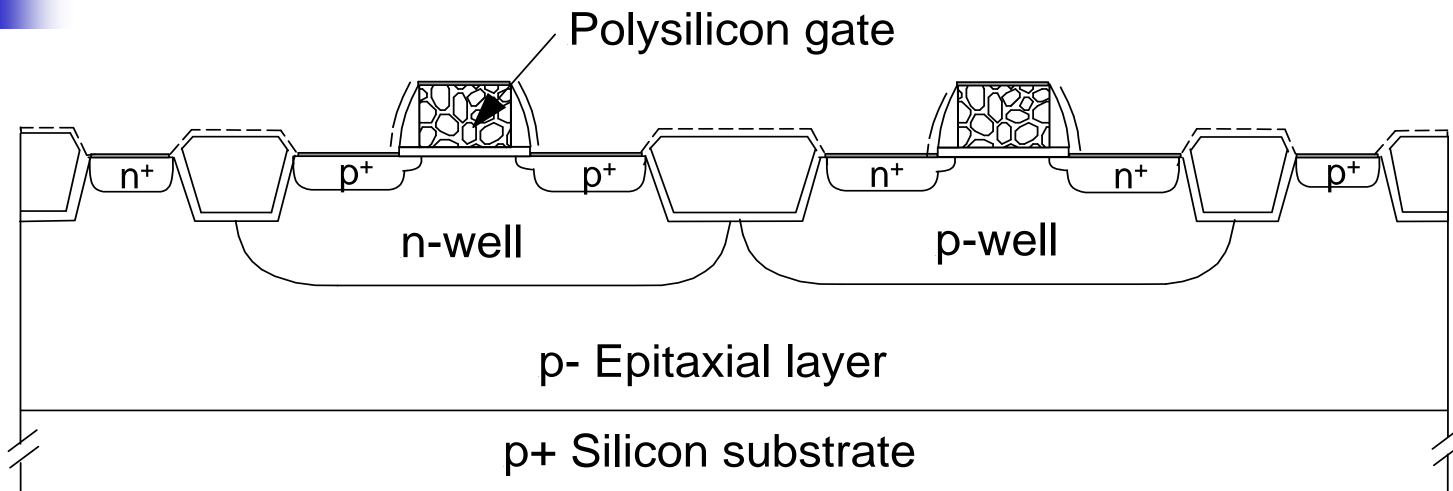
Atmospheric Pressure CVD - Facility

Simple continuous-feed APCVD reactor



Low Pressure CVD (LPCVD) -Applications

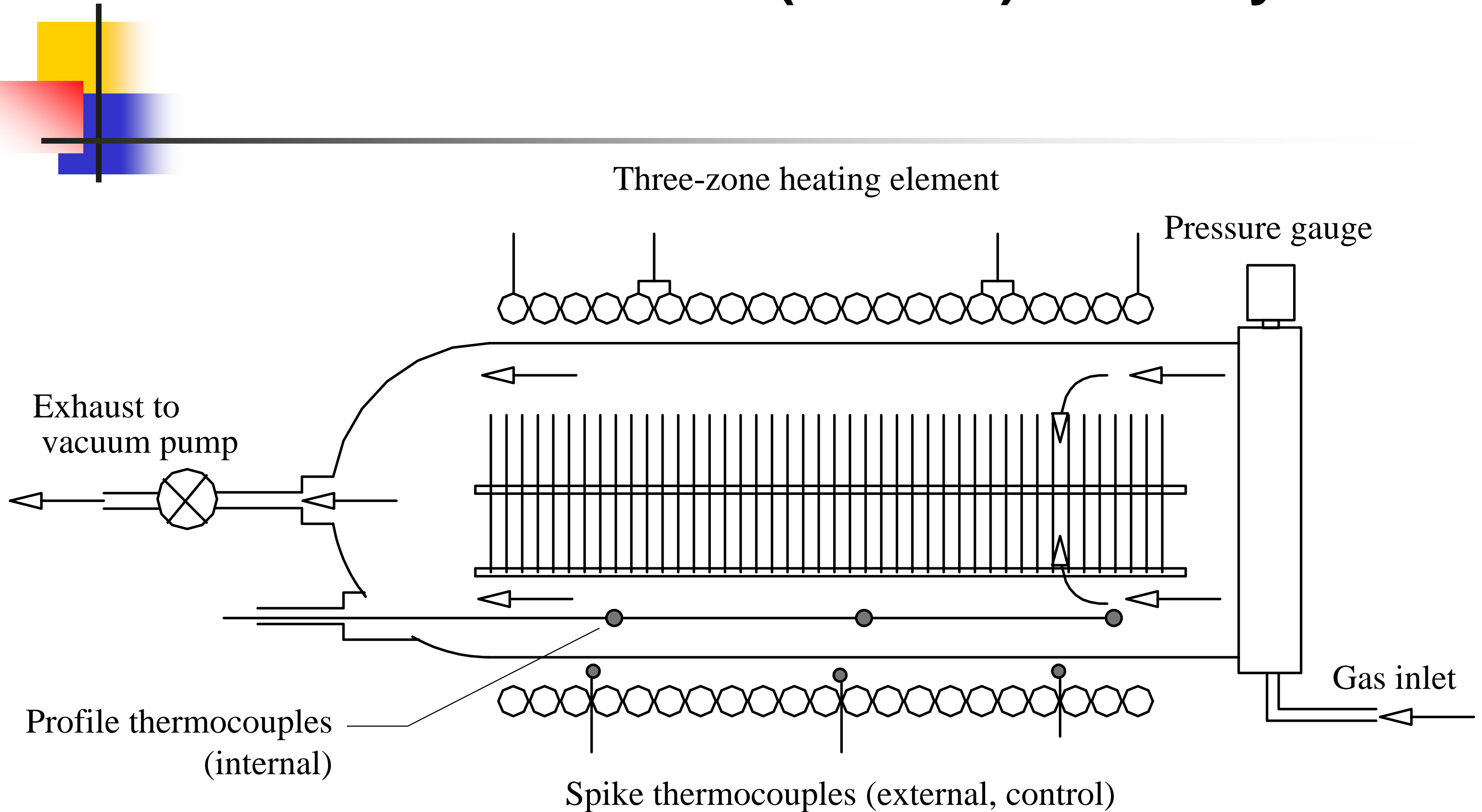
Oxides (TEOS), Nitrides, or Polysilicon



Key Reasons for the Use of Doped Polysilicon in the Gate Structure

1. **Ability to be doped to a specific resistivity.**
2. **Excellent interface characteristics with silicon dioxide.**
3. **Compatibility with subsequent high temperature processing.**
4. **Higher reliability than possible metal electrodes (e.g., aluminum)**
5. **Ability to be deposited conformally over steep topography.**
6. **Allows for self-aligned gate process.**

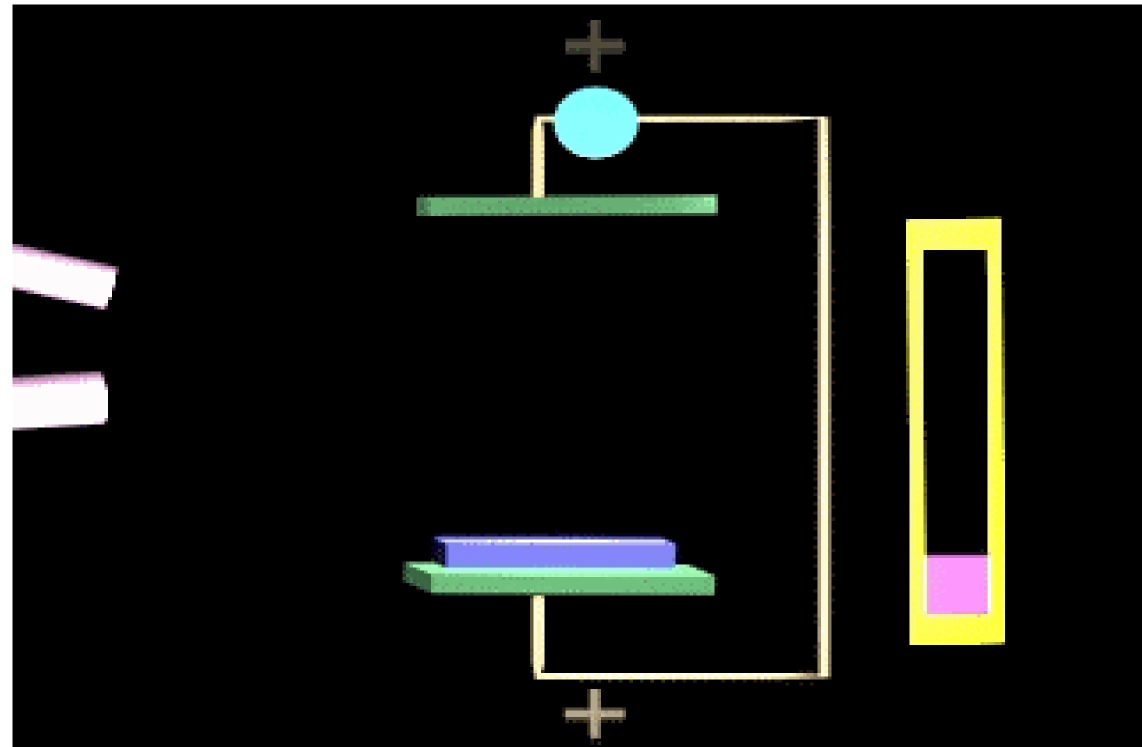
Low Pressure CVD (LPCVD) - Facility



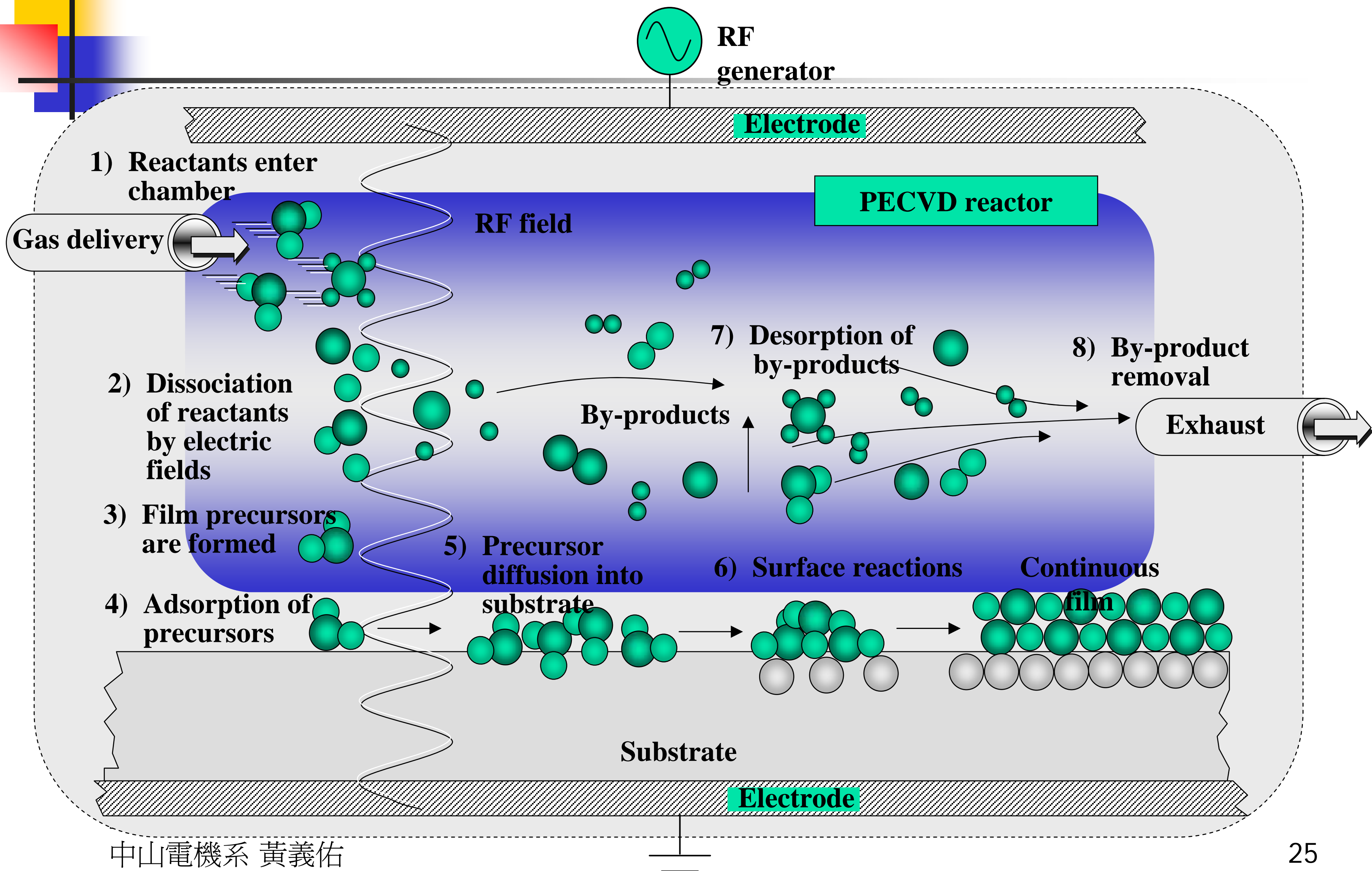
LPCVD Reaction Chamber

Chemical Vapor Deposition

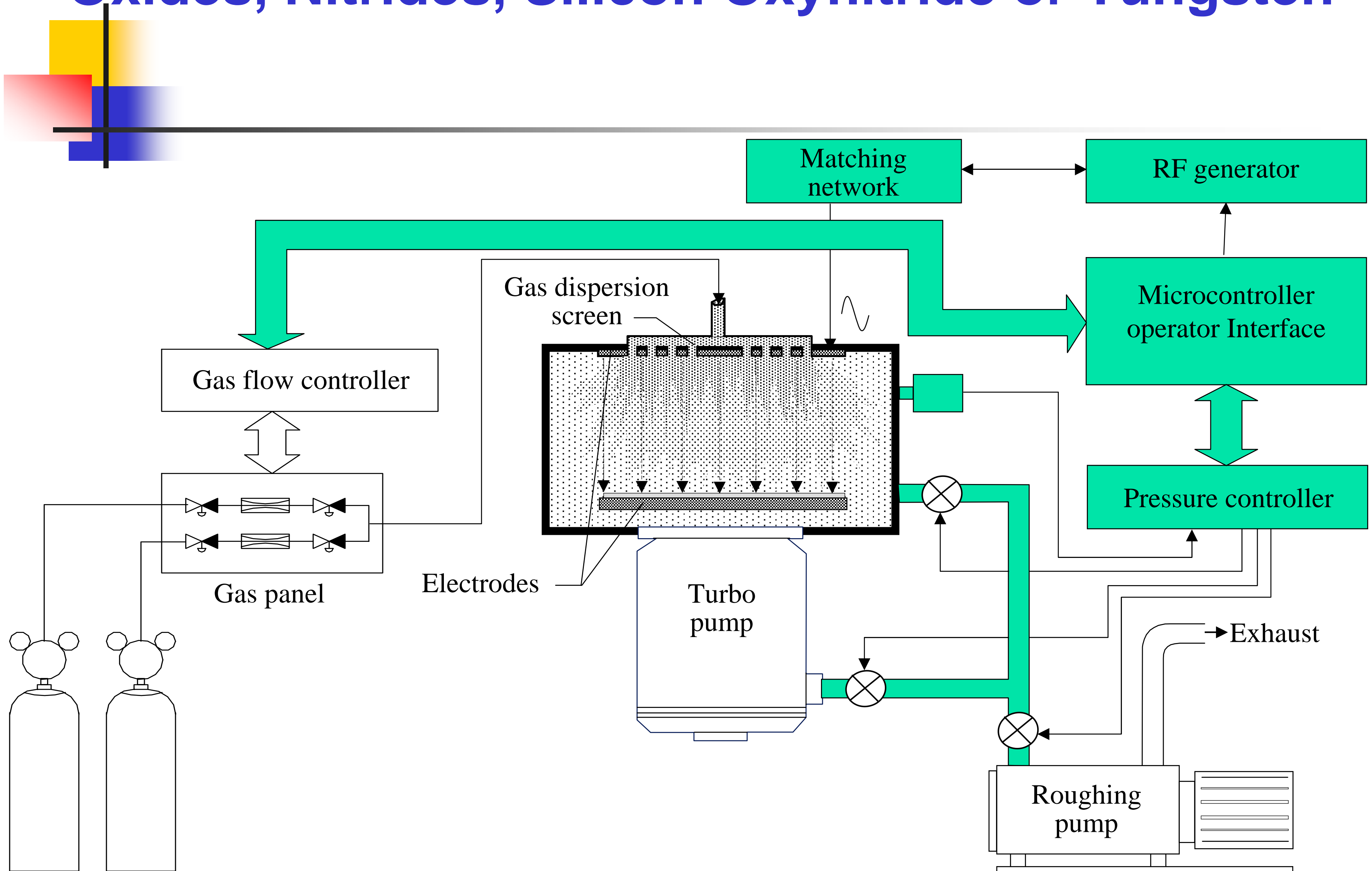
- Plasma Enhanced CVD (PECVD)
  - Induced by high frequency energy



Film Formation during Plasma-Based CVD



General Schematic of PECVD for Deposition of Oxides, Nitrides, Silicon Oxynitride or Tungsten



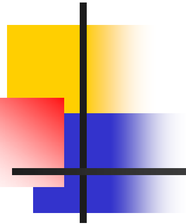
Plasma Enhanced CVD (PECVD)

Properties of Silicon Nitride for LPCVD Versus PECVD

Property	LPCVD	PECVD
Deposition temperature (°C)	700 – 800	300 – 400
Composition	Si_3N_4	$Si_xN_yH_z$
Step coverage	Fair	Conformal
Stress at 23°C on silicon (dyn/cm^{-2})	1.2 – 1.8 x 10^{10} (tensile)	1 – 8 x 10^9 (tensile or compressive)

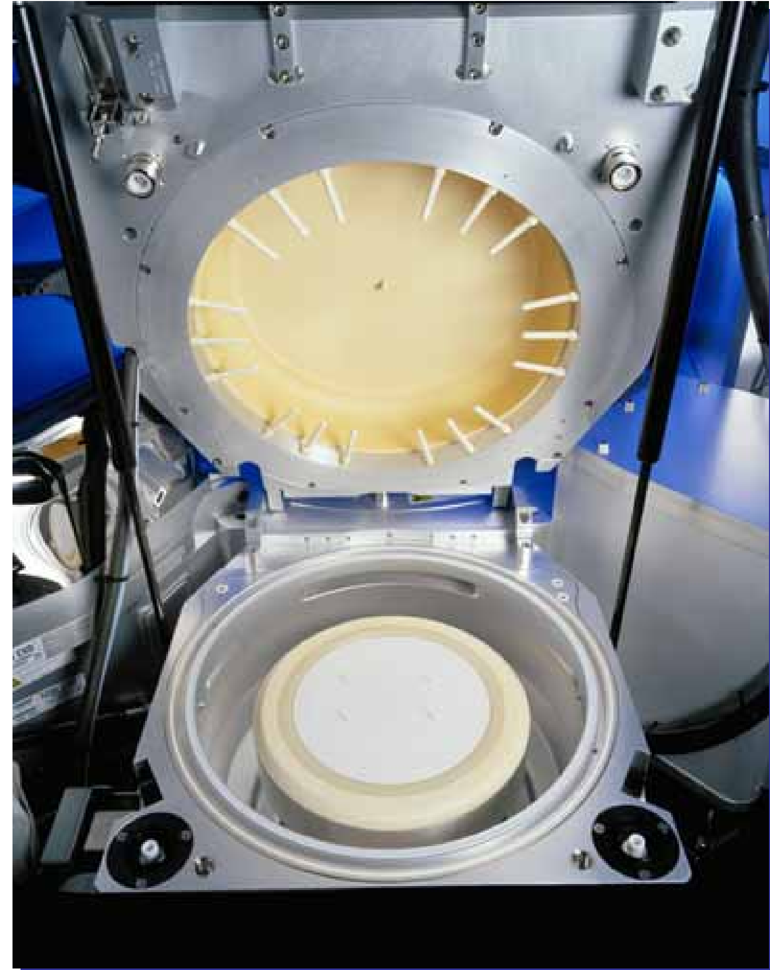
Advantages of Plasma Enhanced CVD

1. Lower processing temperature (250 – 450°C).
2. Excellent gap-fill for high aspect ratio gaps (with high-density plasma).
3. Good film adhesion to the wafer.
4. High deposition rates.
5. High film density due to low pinholes and voids.
6. Low film stress due to lower processing temperature.



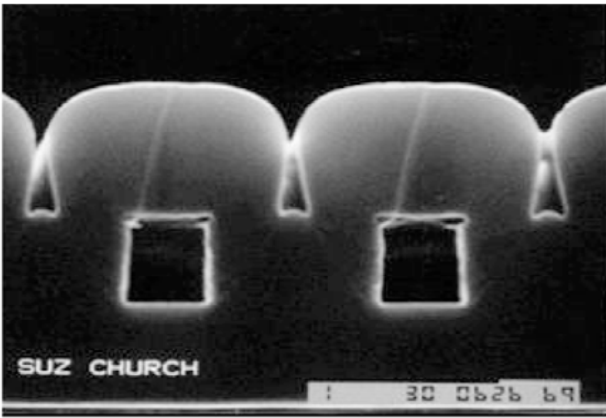
High Density Plasma CVD (HDP CVD)

- Popular in mid-1990s
- High density plasma
- Highly directional due to wafer bias
- Fills high aspect ratio gaps
- Backside He cooling to relieve high thermal load
- Simultaneously deposits and etches film to prevent bread-loaf and key-hole effects

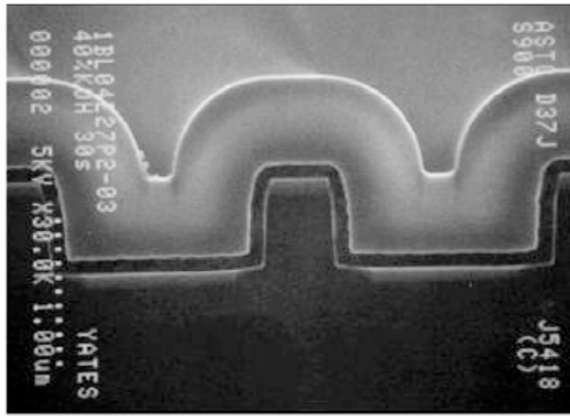


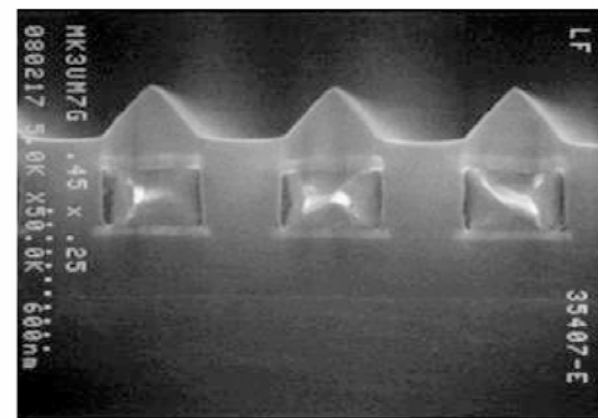
High Density Plasma Deposition Chamber

Profiles of SiO2 deposited by (A) PECVD, (B) LPCVD, and (C) HDPCVD



(A)


(B)


(C)

Bread-loaf effect

SiO_2

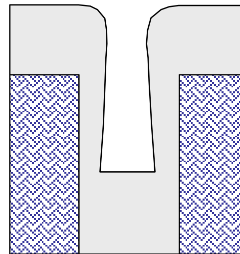
Metal

Key-hole defect (voids)

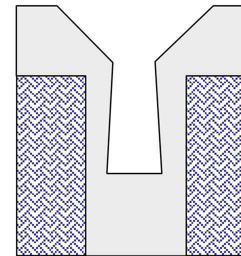
Film deposited with PECVD creates pinch-off at the entrance to a gap resulting in a void in the gap fill.

HDPCVD : Dep-Etch-Dep Process

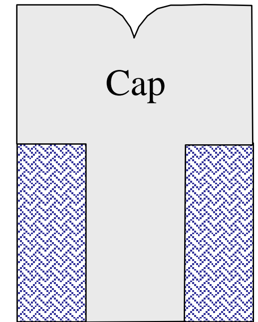
The solution begins here



Ion-induced deposition of film precursors

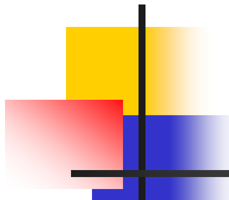


2) Argon ions sputter-etch excess film at gap entrance resulting in a beveled appearance in the film.



3) Etched material is redeposited. The process is repeated resulting in an equal “bottom-up” profile.

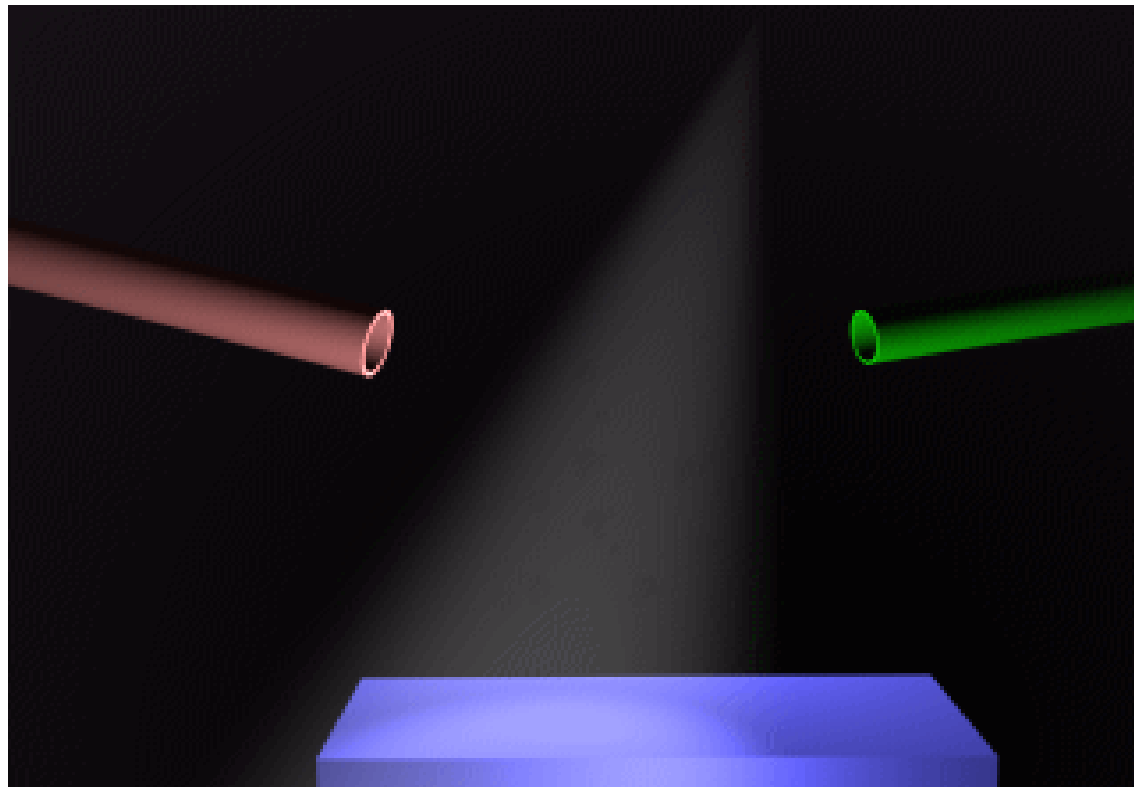
Types of CVD Reactors and Principal Characteristics



Process	Advantages	Disadvantages	Applications
APCVD (Atmospheric Pressure CVD)	Simple reactor, fast deposition, low temperature.	Poor step coverage, particle contamination, and low throughput.	Low-temperature oxides (both doped and undoped).
LPCVD (Low Pressure CVD)	Excellent purity and uniformity, conformal step coverage, large wafer capacity.	High temperature, low deposition rate, more maintenance intensive and requires vacuum system.	High-temperature oxides (both doped and undoped), silicon nitride, polysilicon, W, WSi_2.
Plasma Assisted CVD: ▪ Plasma Enhanced CVD (PECVD) ▪ High Density Plasma CVD (HDPCVD)	Low temperature, fast deposition, good step coverage, good gap fill.	Requires RF system, higher cost, stress is much higher with a tensile component, and chemical (e.g., H_2) and particle contamination.	High aspect ratio gap fill, low-temperature oxides over metals, ILD-1, ILD, copper seed layer for dual damascene, passivation (nitride).

Chemical Vapor Deposition

- Photon Induced CVD (PHCVD)
  - Induced by light



Metal CVD - Copper Electroplating

- Cathode

Outlet

Copper atom attached to wafer

Substrate

Outlet

Copper ion

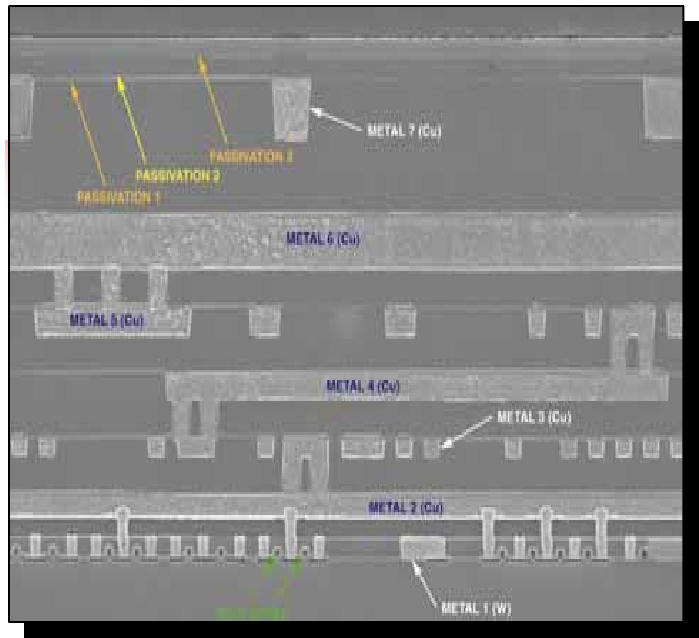
Plating solution

+ Copper anode

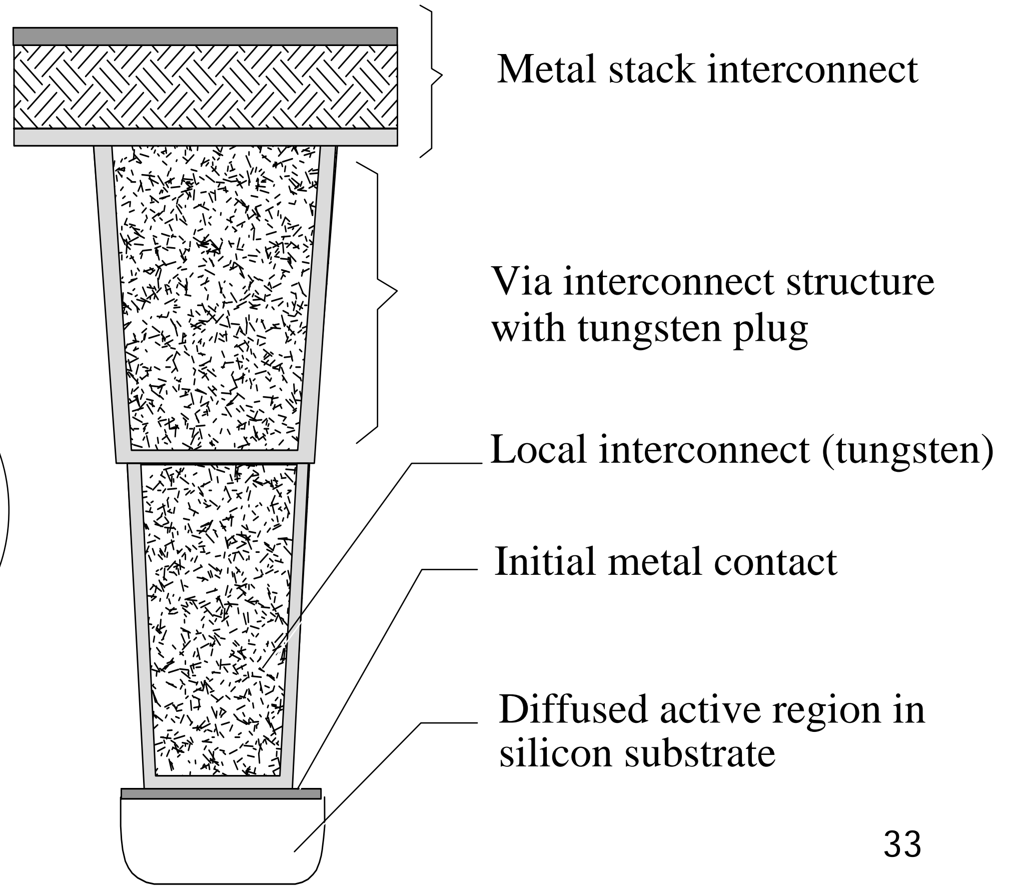
Inlet

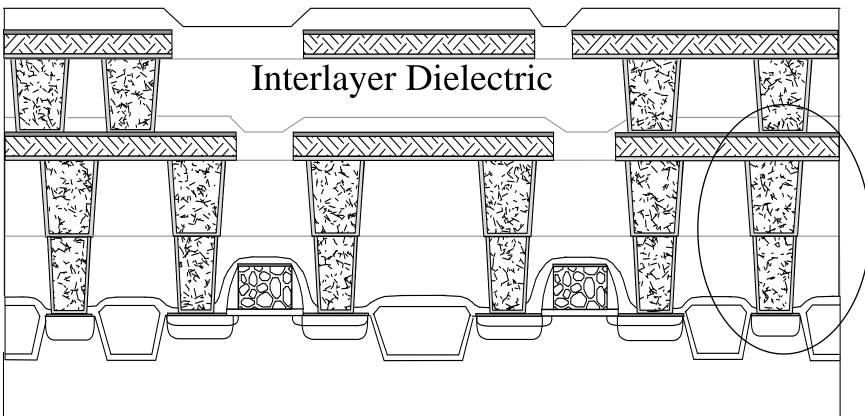
Used with permission from Novellus Systems, Inc.

Overview of Multilevel Metallization



Metal interconnect structure



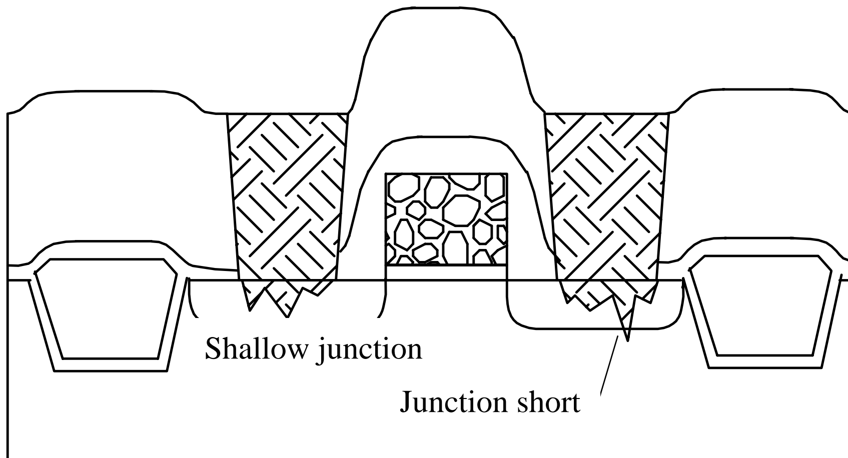


Sub quarter micron CMOS cross section

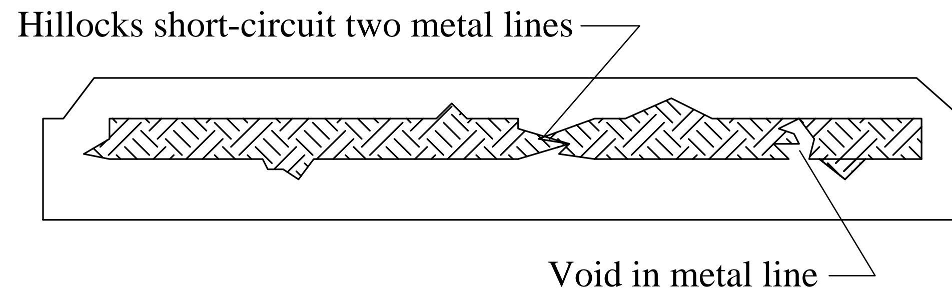
Aluminum Interconnect

Bonding pad Metal-5
(Aluminum)
Top Nitride
ILD-6
Metal-4
ILD-5
Via-4
Metal-3
ILD-4

Metal-4 is preceded by other vias, interlayer dielectric, and metal layers.



Junction Spiking



Hillock on a Metal Line due to Electromigration

Copper Metallization

The Benefits of Copper Interconnect:

1. Reduction in resistivity -- 1.678 $\mu\Omega$-cm (Cu) vs. 2.65 $\mu\Omega$-cm (Al)
2. Reduction in power consumption
3. Tighter packing density
4. Superior resistance to electromigration
5. Fewer process steps -- 20 to 30 % fewer steps with damascene technique

Comparison of Properties/Processes Between Al and Cu

Property/Process	Al	Cu
Resistivity ($\mu\Omega$-cm)	2.65 (3.2 for Al-0.5%Cu)	1.678
Electromigration resistance	Low	High
Corrosion resistance (in air)	High	Low
Etch processing	Yes	No
CMP (chemical mechanical planarization) processing	Yes	Yes

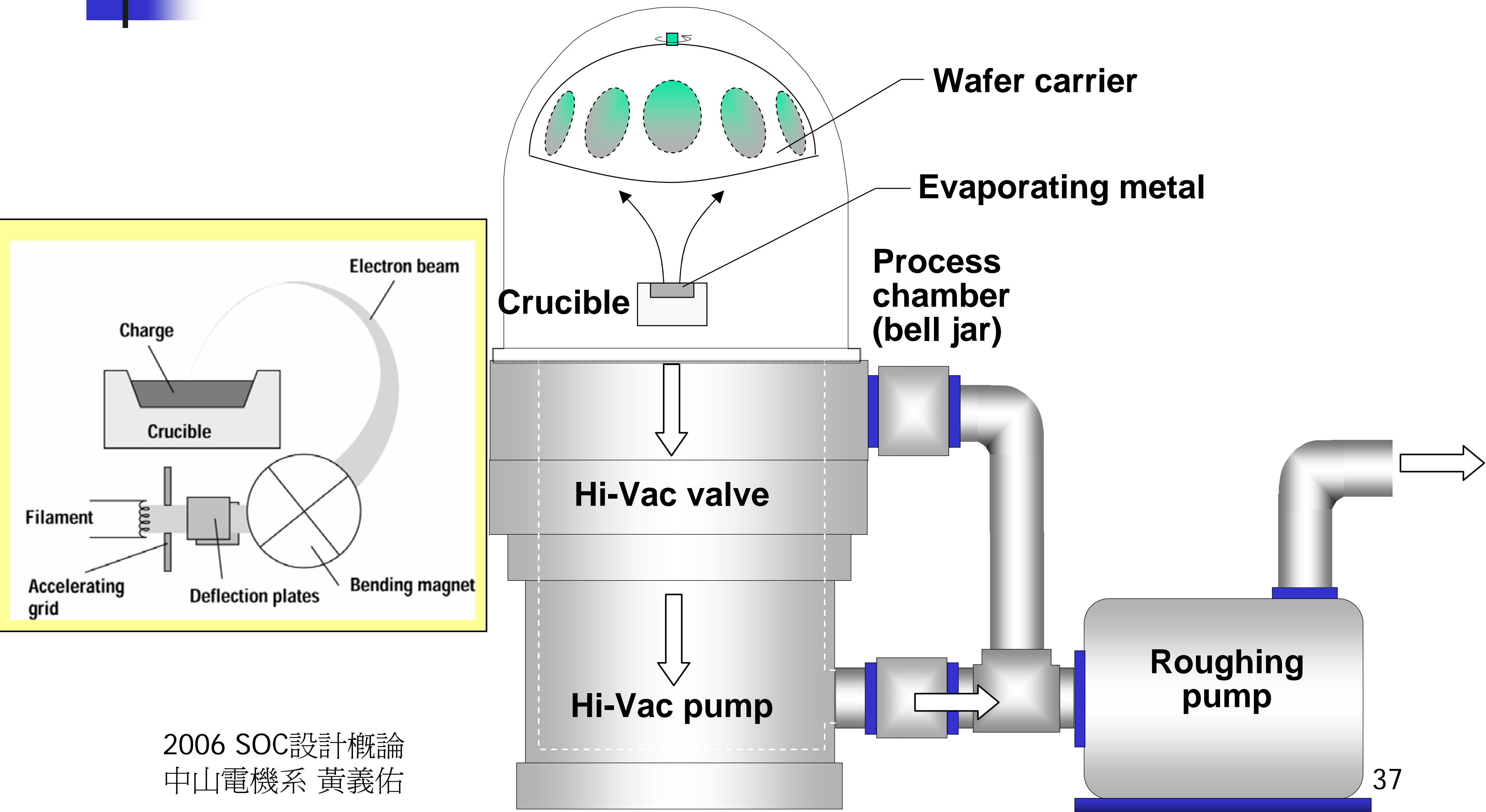
Silicon and Select Wafer Fab Metals (at 20°C)

Material	Melting Temperature (°C)	Resistivity ($\mu\Omega$-cm)
Silicon (Si)	1412	$\approx 10^9$
Doped Polysilicon (Doped Poly)	1412	≈ 500 – 525
Aluminum (Al)	660	2.65
Copper (Cu)	1083	1.678
Tungsten (W)	3417	8
Titanium (Ti)	1670	60
Tantalum (Ta)	2996	13 – 16
Molybdenum (Mo)	2620	5
Platinum (Pt)	1772	10

Metal Deposition Systems
- Physical Vapor Deposition (PVD)

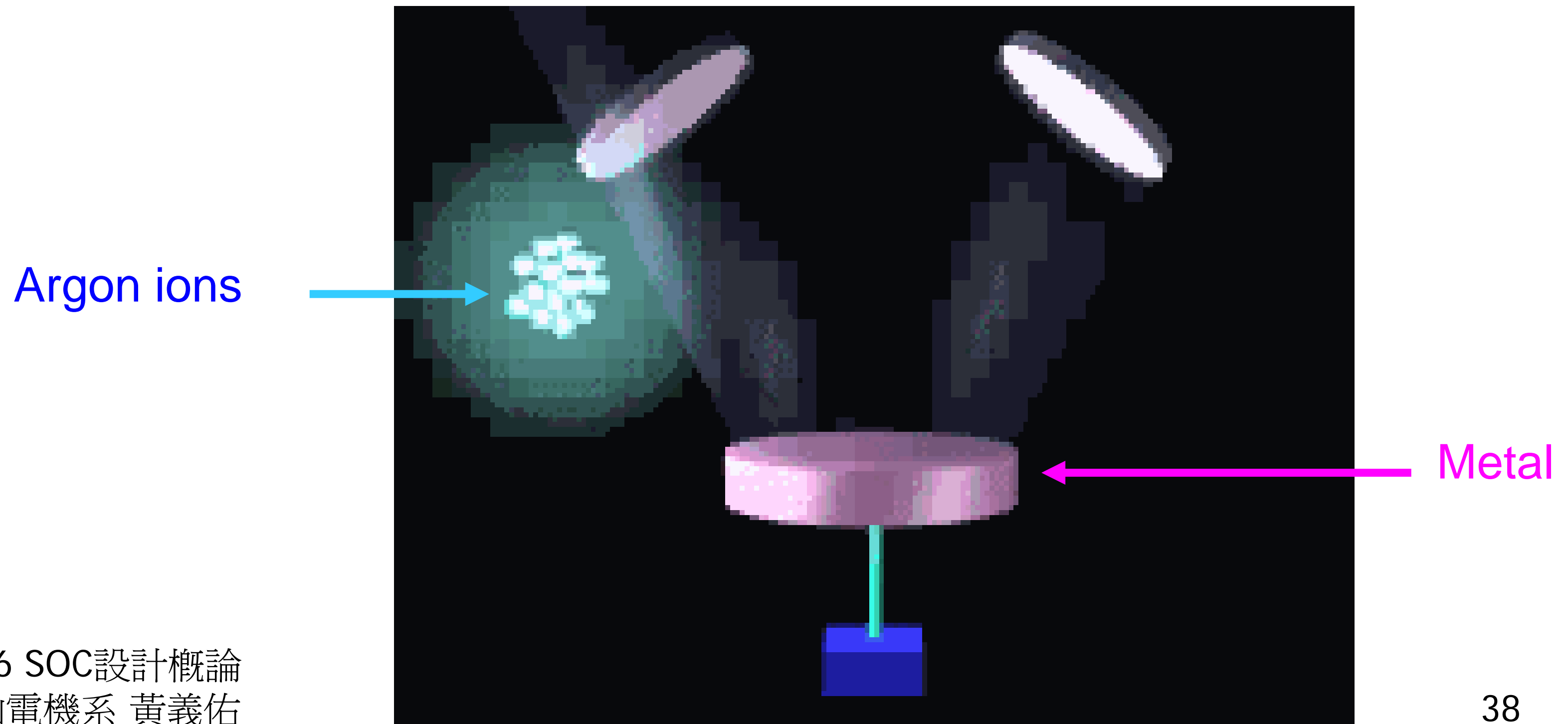
E-beam Evaporator

- Evaporation
- Sputtering
- Metal CVD
- Copper electroplating



Sputter Deposition

- Sputter Process
  - Metal films are used in IC fabrication
    - Argon gas is excited by a high energy field



Metal Deposition Systems
- Physical Vapor Deposition (PVD)

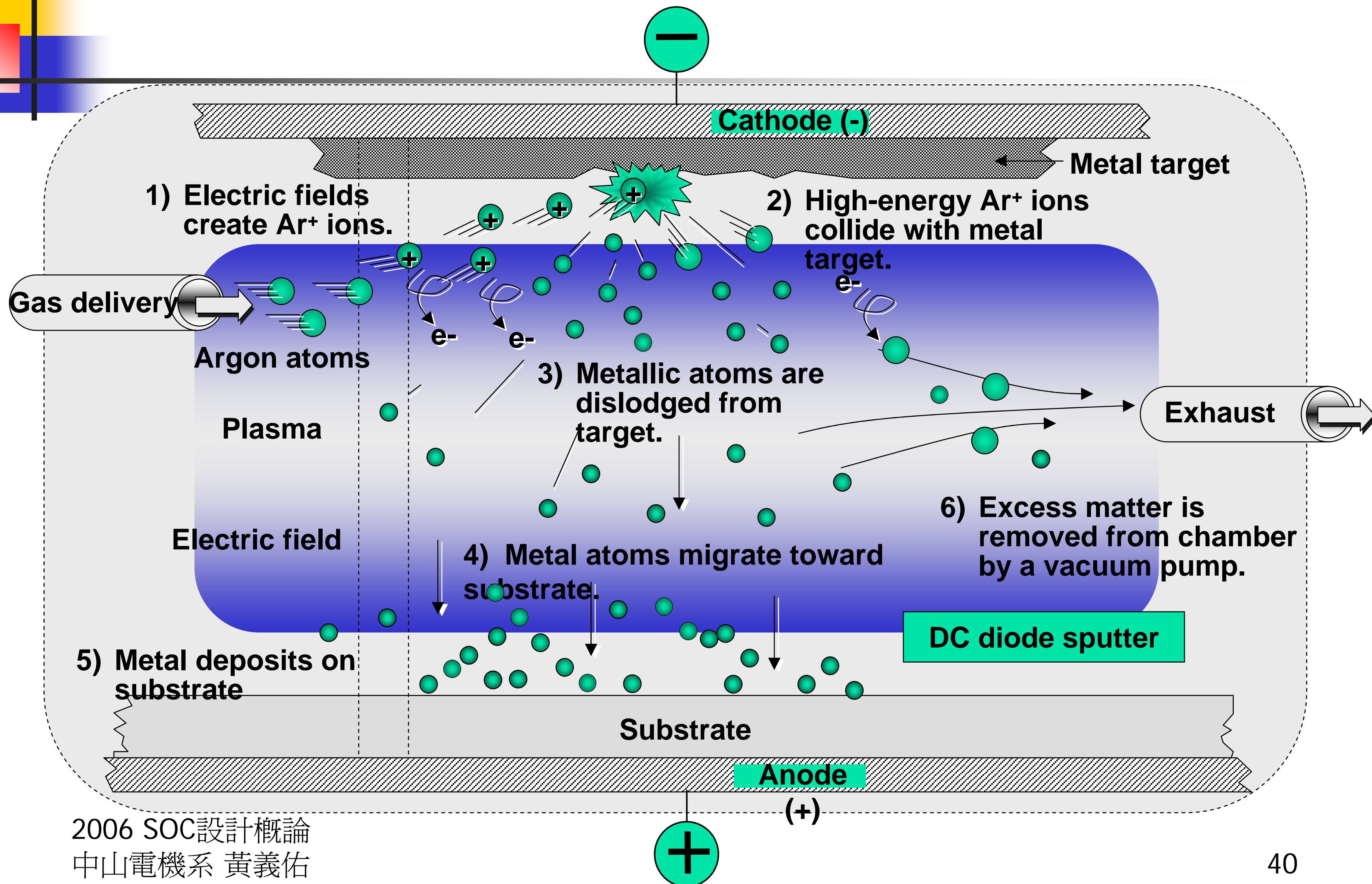
Sputtering

Some Advantages of Sputtering

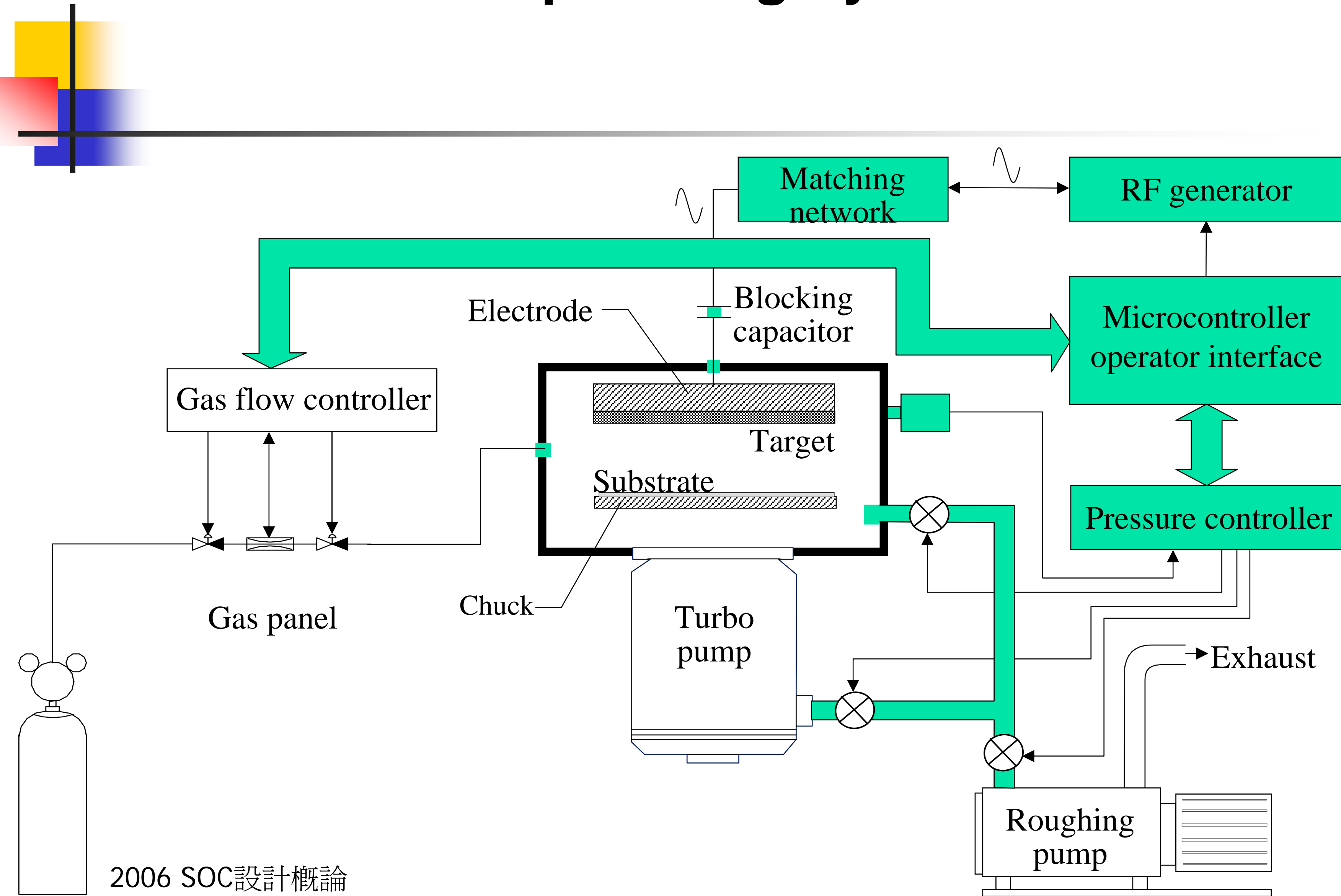
1. Ability to deposit and maintain complex alloys.
2. Ability to deposit high-temperature and refractory metals.
3. Ability to deposit controlled, uniform films on large wafers (200 mm and larger).
4. Ability of multichamber cluster tools to clean the wafer surface for contamination and native oxides before depositing metal (referred to as in situ sputter etch).

Photo Courtesy of Applied Materials, Inc.

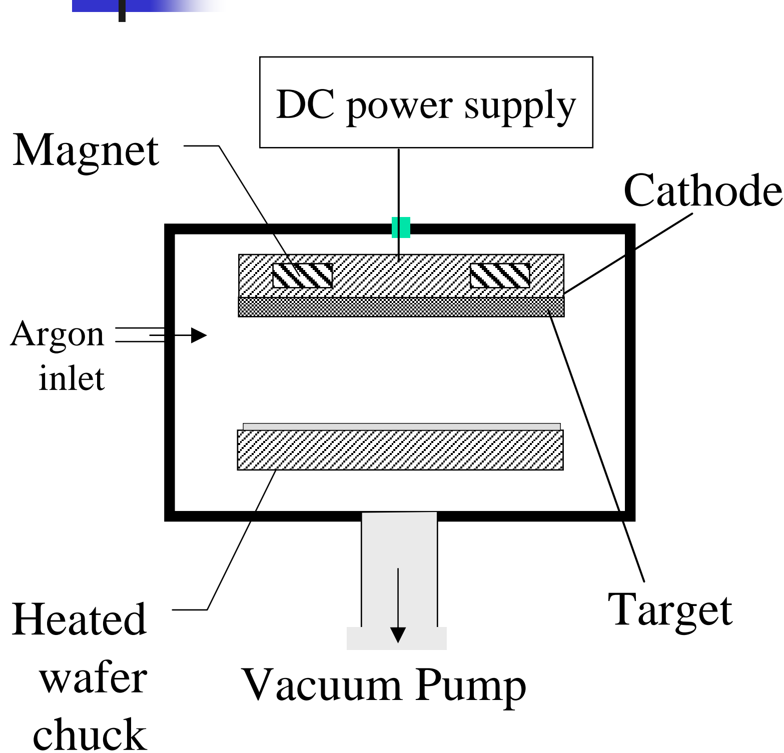
Simple Parallel Plate DC Diode Sputtering System

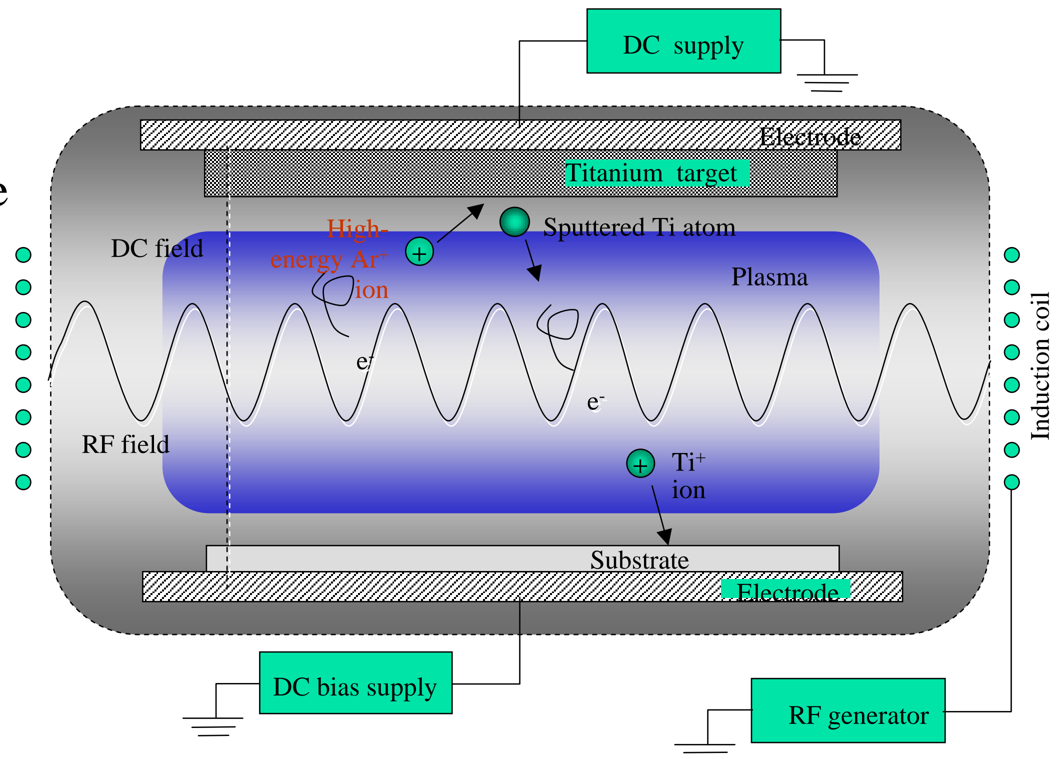


RF Sputtering Systems



Magnetron & Ionized Metal Plasma Sputtering Systems





Magnetron Sputtering

Ionized Metal Plasma (IMP) PVD

液相磊晶(LPE)

- 熱平衡狀態下成長
- 採用材料熔點會因不同材料混合時熔點下降之特點

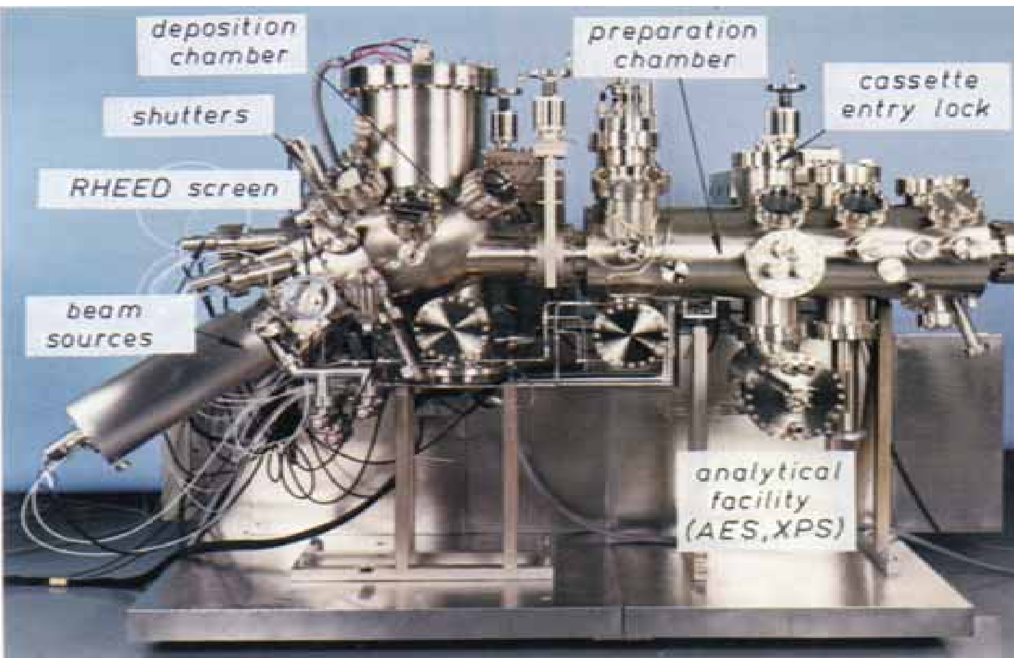
  Example : GaAs (m.p.= 1238°C)

  GaAs+Ga (m.p.<< 1238 °C)
- 優點: 產量大，成本較低，成長速度快
- 缺點: 無法精確控制薄膜厚度，無法成長極薄之薄膜，無法成長多樣式不同成分之薄膜，界面分野較不清楚

氣相磊晶(VPE)

- 非熱平衡狀態下成長
- 材源以氣相方式滯留在基底(substrate)附近，藉基底之熱源將該材源給予熱解，進而沈積在基底表面。
- 材源可以有多樣化，氣體或液體均可。
- 藉由流量控制器控制成長速度，因此薄膜厚度的掌控，可以相當精準
- 所使用之氣體，通常含有劇毒，在安全方面的考量，須較為慎重。
- 薄膜成長速度快，產量大，為業界的寵兒。
- 基於材源的多樣性，不限於半導體薄膜的成長，各種材料均可適用

分子束磊晶 (MBE)



- 利用超高真空環境將高純度材源由固體加熱成氣體，隨即該氣體成為所謂分子束以熱能為其運動能移動至基底上形成薄膜。
- 儀器造價昂貴
- 薄膜品質遠較其他成長方法優良
- 能在極低之溫度下成長薄膜，同時依舊保有優良品質
- 在相關儀器的配合下能夠達到動態控制薄膜厚度的控制成長。
- 保有防止其他雜質污染的最大優點。
- 成長速度慢，量產不易，大都用來成長特殊高附加價值之半導體薄膜。
- 改良式的儀器可利用液體極氣體之材源，增加該方法的適用範圍。
- 由於在超高真空環境之下，有助於表面科學對於薄膜成長的研究
- 配合其他真空腔體的結合，容易達到所謂一貫作業的處理系統