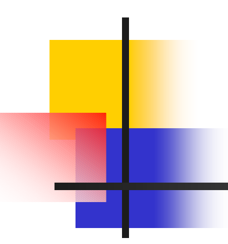
Chapter 3 : ULSI Manufacturing Technology – (a) Oxidation & Impurity Doping

Reference

1. **Semiconductor Manufacturing Technology*: Michael Quirk and Julian Serda (2001)***
2. 國家矽導計畫-教育部晶片法商學程編定教材
3. **ULSI Technology *: C. Y. Chang, S. M. Sze (1996)***
4. **Semiconductor Physics and Devices- Basic Principles (3/e) *: Donald A. Neamen (2003)***
5. **Semiconductor Devices *- Physics and Technology* (2/e) *: S. M. Sze (2002)***

Stages of IC Fabrication



1.	**Wafer Preparation** includes crystal growing, rounding, slicing and polishing. Single crystal silicon Wafers sliced from ingot	4.	**Assembly and Packaging:** The wafer is cut along scribe lines to separate each die. Scribe line A single die
2.	**Wafer Fabrication** includes cleaning, layering, patterning, etching and doping.	5.	Metal connections are made and the chip is encapsulated. Assembly Packaging
3.	**Test/Sort** includes probing, testing and sorting of each die on the wafer. Defective die		**Final Test** ensures IC passes electrical and environmental testing.

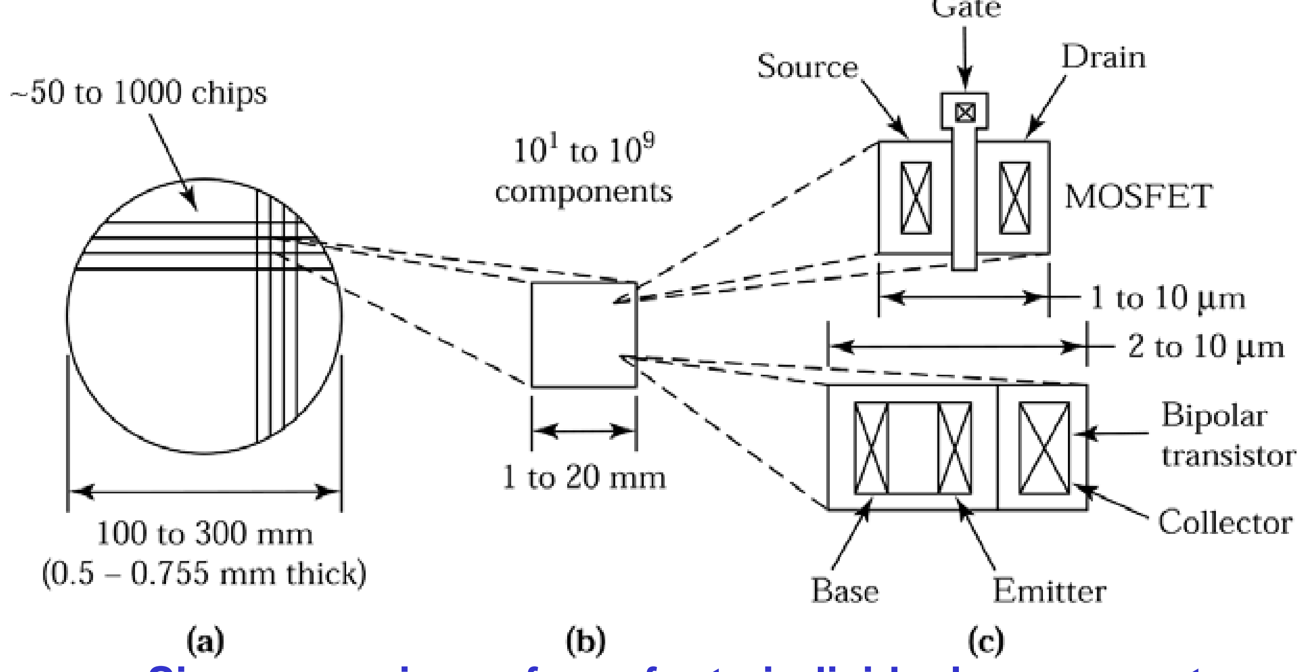
Evolution of IC Technology

積體電路技術的發展概況

年 份	1989	1992	1995	1998	2001
最小線寬	0.7	0.5	0.35	0.25	0.18
電晶體數量	—	300 K	800 K	2 M	5 M
DRAM 容量	4 MB	16 MB	64 MB	256 MB	2 GB
邏輯電路大小 (mm^2)	—	250	400	600	800
DRAM 大小 (mm^2)	—	132	200	320	500
晶片直徑 (mm)	150	150 ~ 200	200	200 ~ 300	300 ~ 400

積體電路 MOS 技術的發展概況

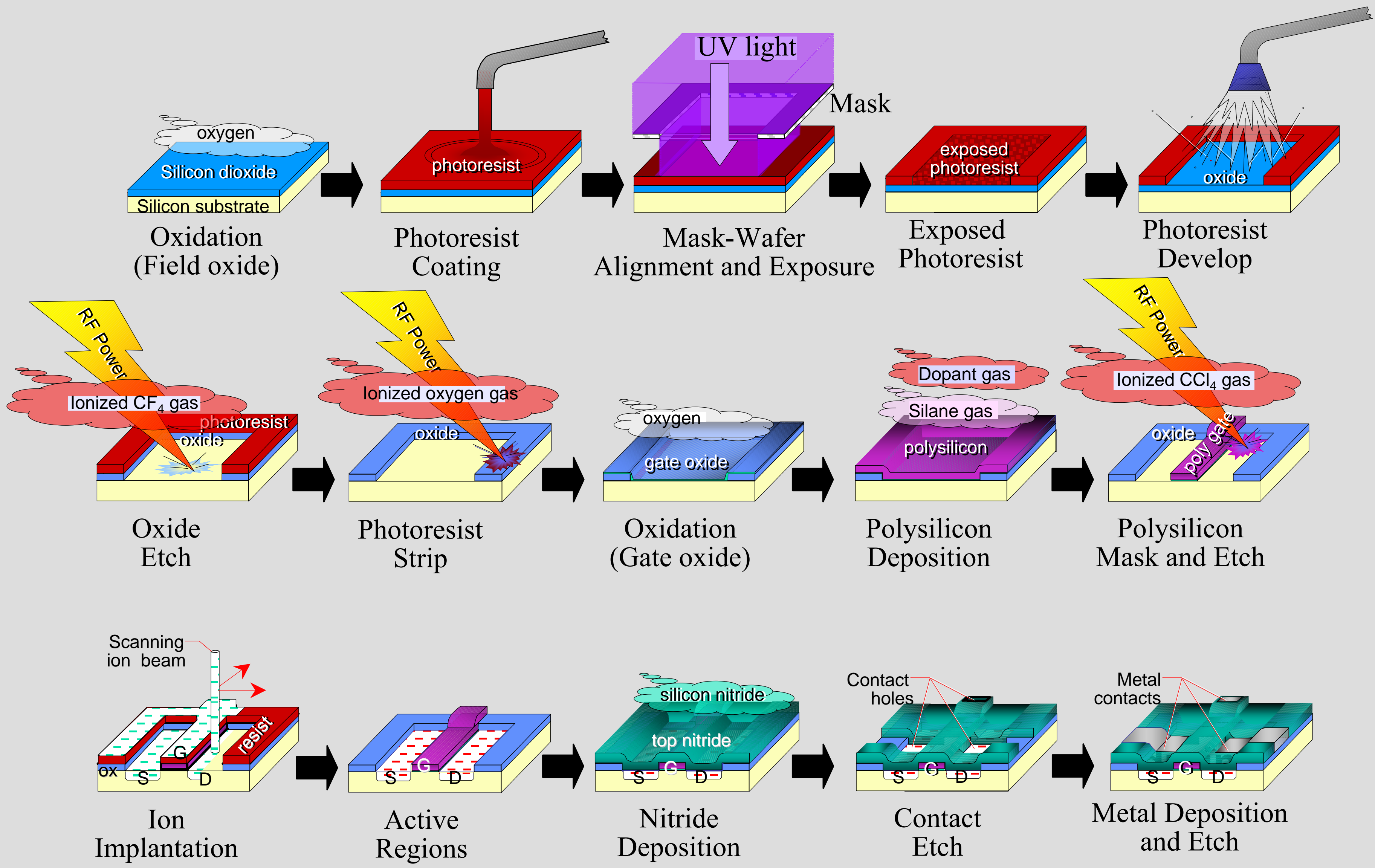
年 份	1980	1989	1992	1995	1998	2001
MOS 閘厚度 (Å)	400	200	150	90	80	70
MOS 閘長度 (μm)	2	0.9 ~ 0.8	0.6 ~ 0.5	0.4 ~ 0.3	0.25	0.18
MOS 接合深度 (μm)	0.6	0.2	0.15	0.15	0.1	0.08
Vcc 電壓 (V)	5	5	5 →	3.3	3.3	3.3
NMOS I_{dsat} (mA / μm)	0.14	0.36	00.56	0.48	0.55	0.65
PMOS I_{dsat} (mA / μm)	0.06	0.19	0.27	0.22	0.26	0.32



Size comparison of a wafer to individual components.
(*a*) Semiconductor wafer. (*b*) Chip. (*c*) MOSFET and bipolar transistor.

IC Fabrication Process Overview

Major Fabrication Steps in MOS Process Flow



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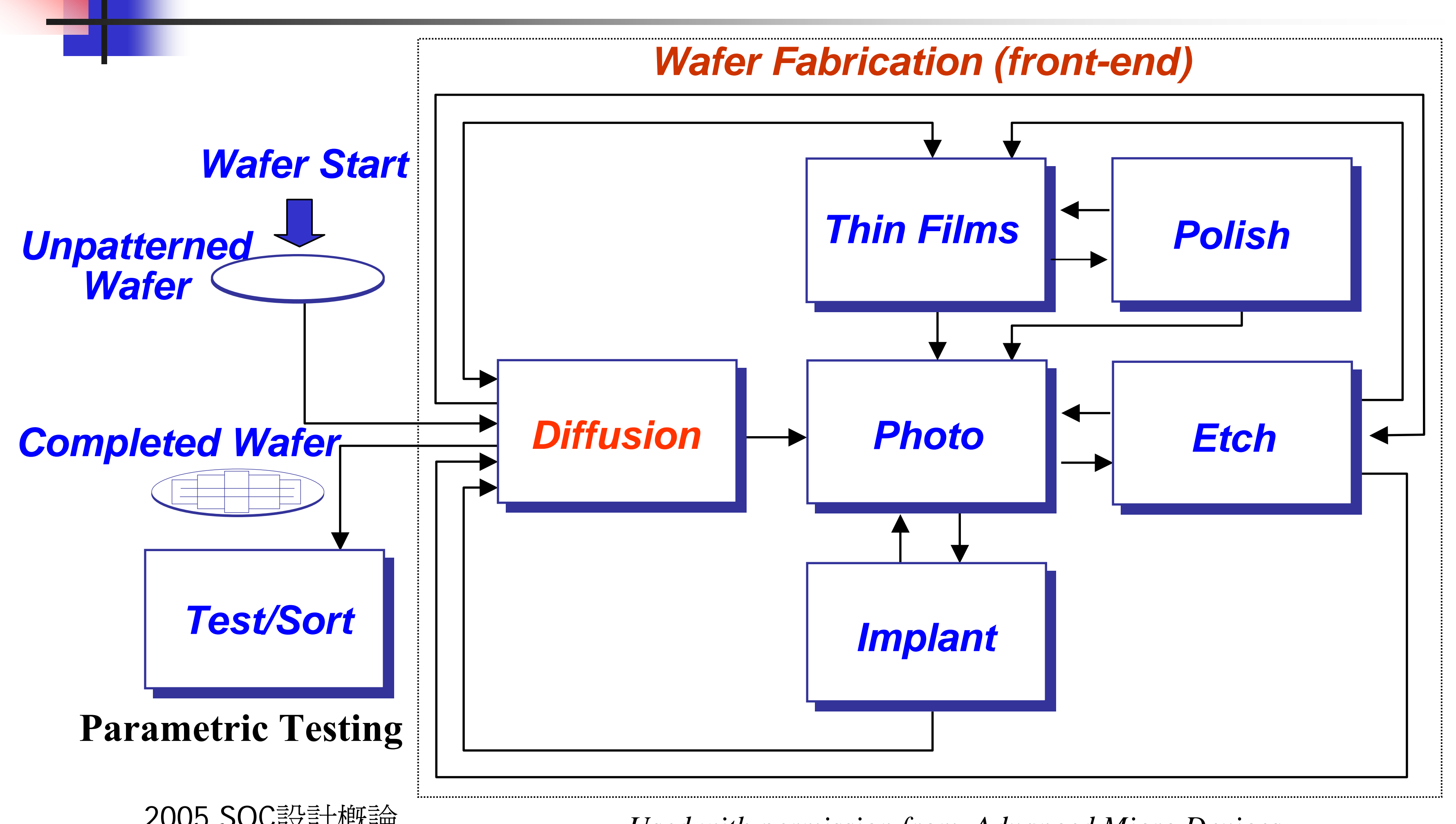
Model of Typical Wafer Flow in a Sub-Micron CMOS IC Fab



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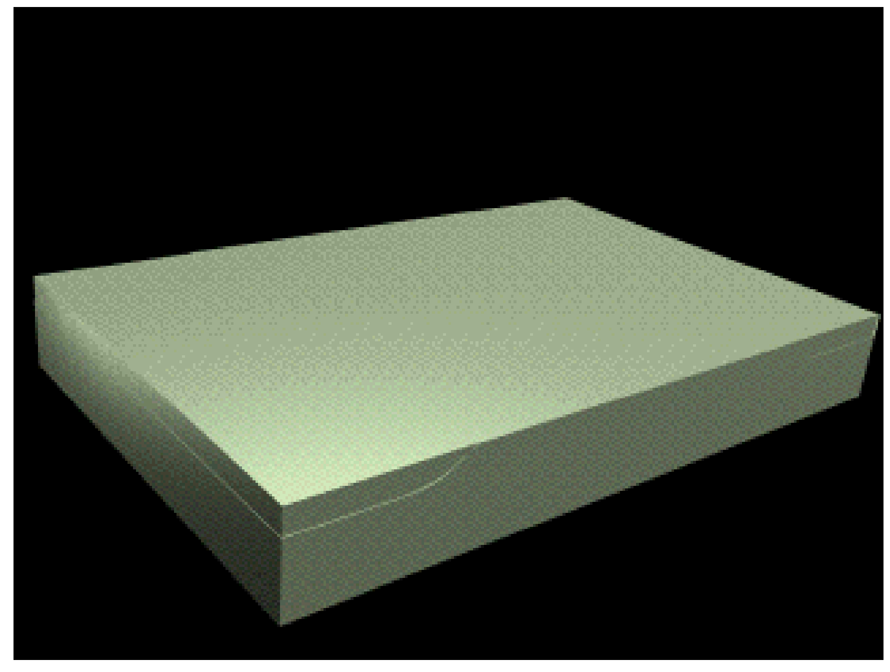
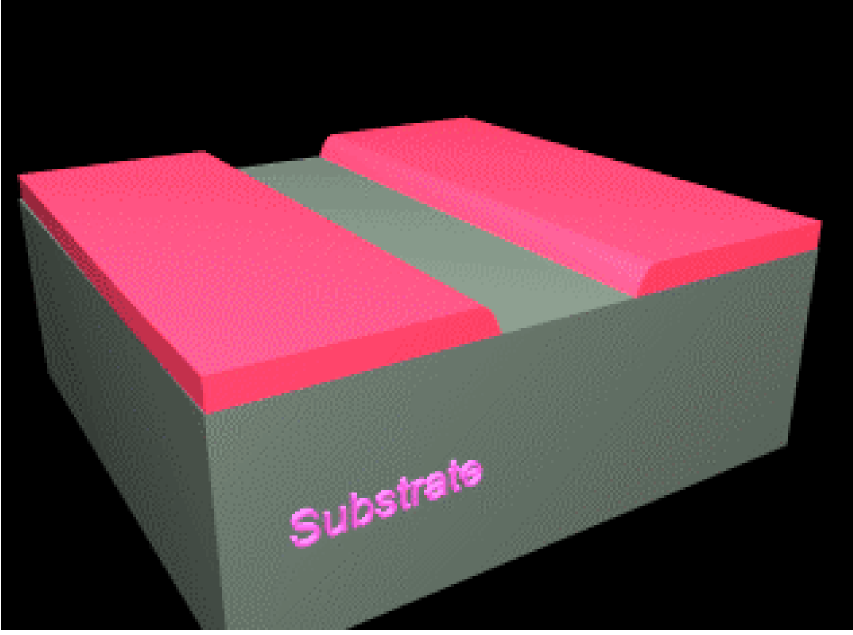
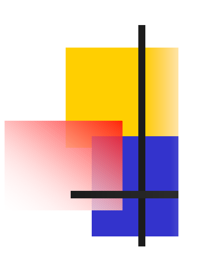
Oxidation

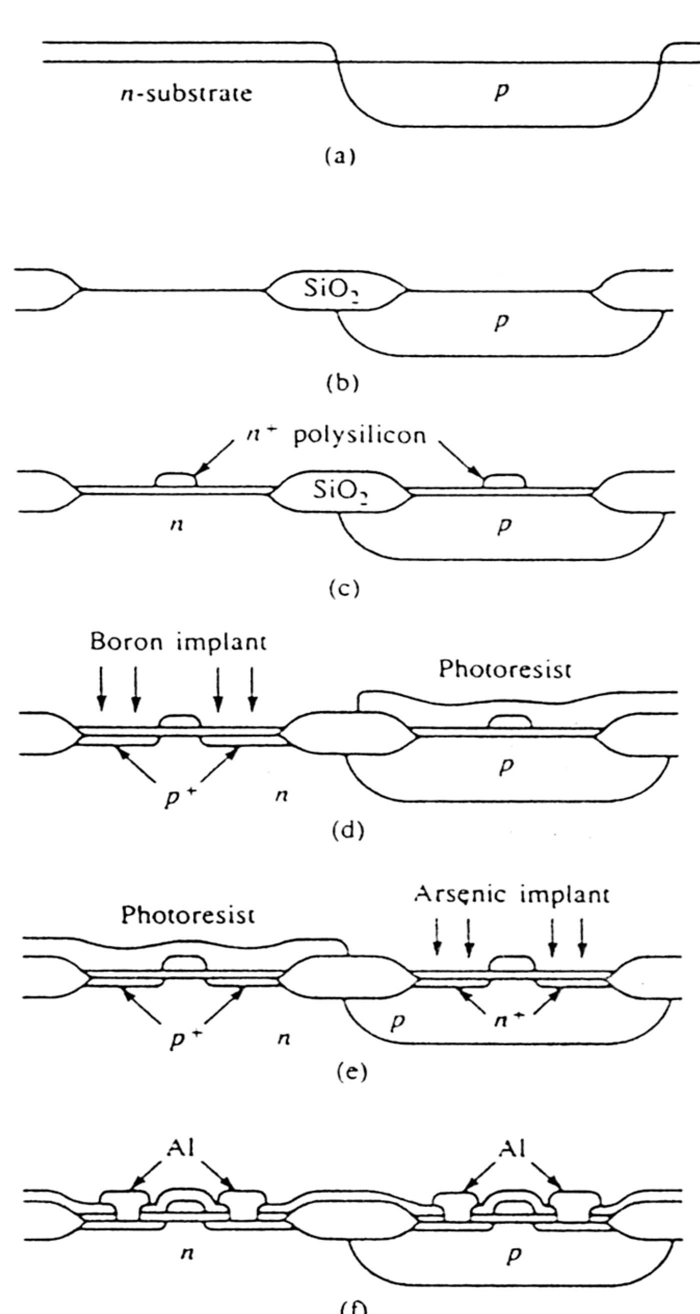
- **Object**
  - **Gate dielectric**
  - **Protective coating in many steps of fabrication**

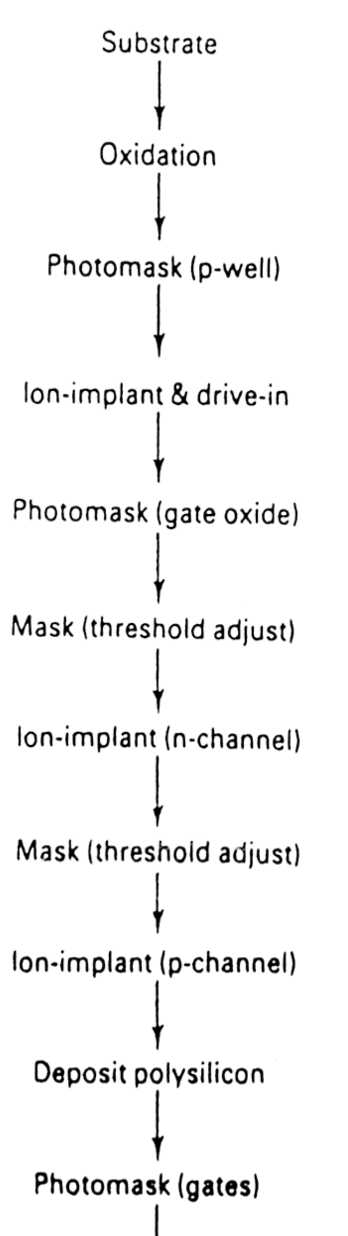


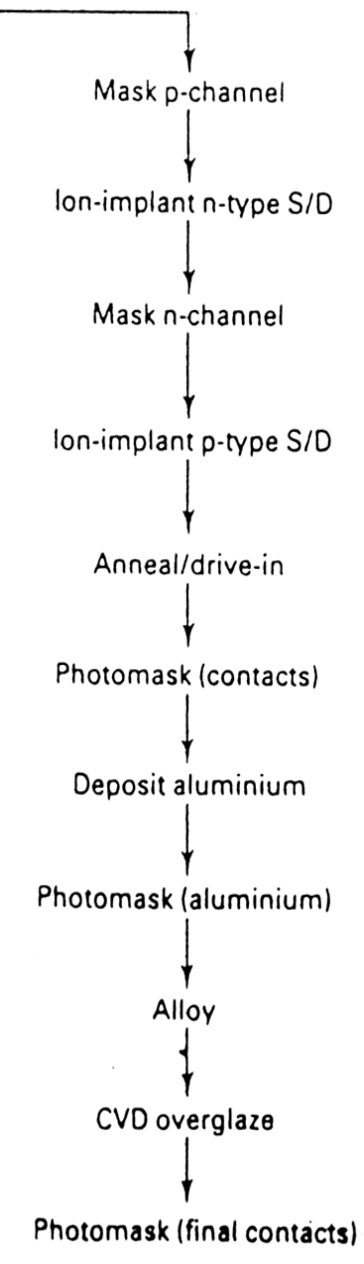


A Basic CMOS Process









Oxide Applications

Native Oxide

p+ Silicon substrate

Purpose: This oxide is a contaminant and generally undesirable

Comments: Growth rate at 300K is 15 per hour up to about 40 Å.

Field Oxide

Transistor site

p+ Silicon substrate

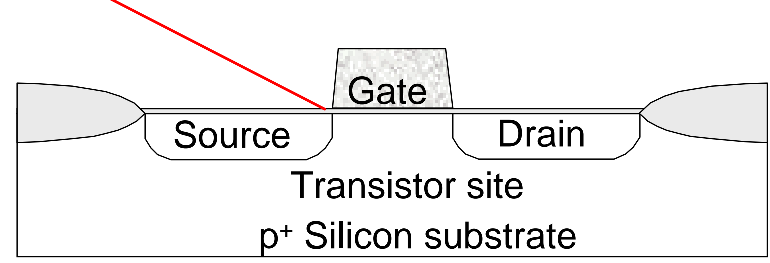
Purpose: Serves as an isolation barrier between individual transistors to isolate them from each other.

Comments: Common film thickness : 2,500 Å ~ 15,000 Å.
Wet oxidation is the preferred method.

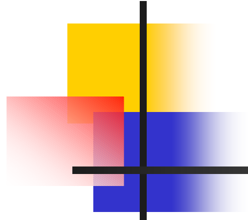
Gate Oxide

Purpose: Serves as a dielectric between the G and S/D parts of MOSFET

Comments: Common film thickness : 20 Å ~ 600 Å (0.18 μm process)
Dry oxidation is the preferred method.



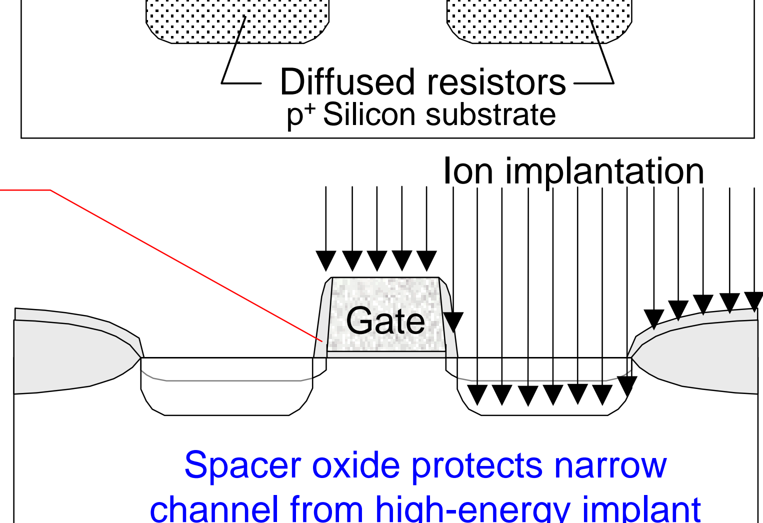
Oxide Applications



Barrier Oxide

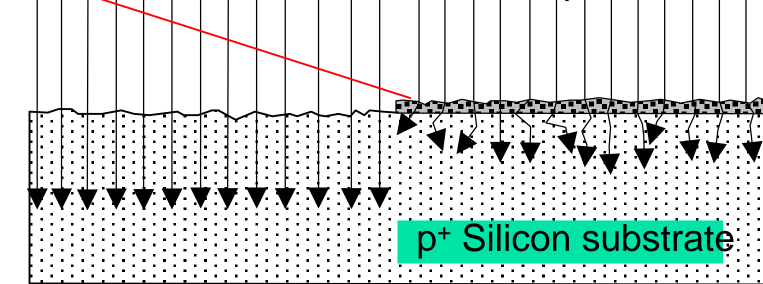
Purpose: Protect active devices and silicon from follow-on processing.
Common film thickness : 150 Å
Comments: Thermally grown to several hundred Angstroms thickness.

Dopant Barrier



Purpose: Masking material when implanting dopant into wafer.
Common film thickness : 400 ~ 1200 Å
Example: Spacer oxide used during the implant of dopant into the source and drain regions.
Comments: Dopants diffuse into unmasked areas of silicon by selective diffusion.

Implant Screen Oxide



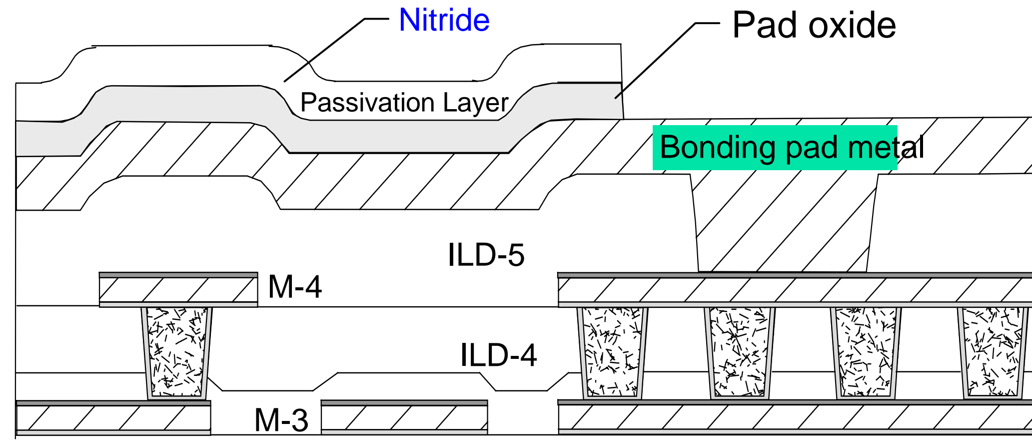
Purpose: Sometimes referred to as "sacrificial oxide", screen oxide, is used to reduce implant channeling and damage.
Assists creation of shallow junctions.
Thickness varies depending on dopant, implant energy, time
Comments: Thermally grown

Oxide Applications

Pad Oxide

Purpose: Provides stress reduction for Si_3N_4
Common film thickness : 200 ~ 500 Å

Comments: Thermally grown and very thin.



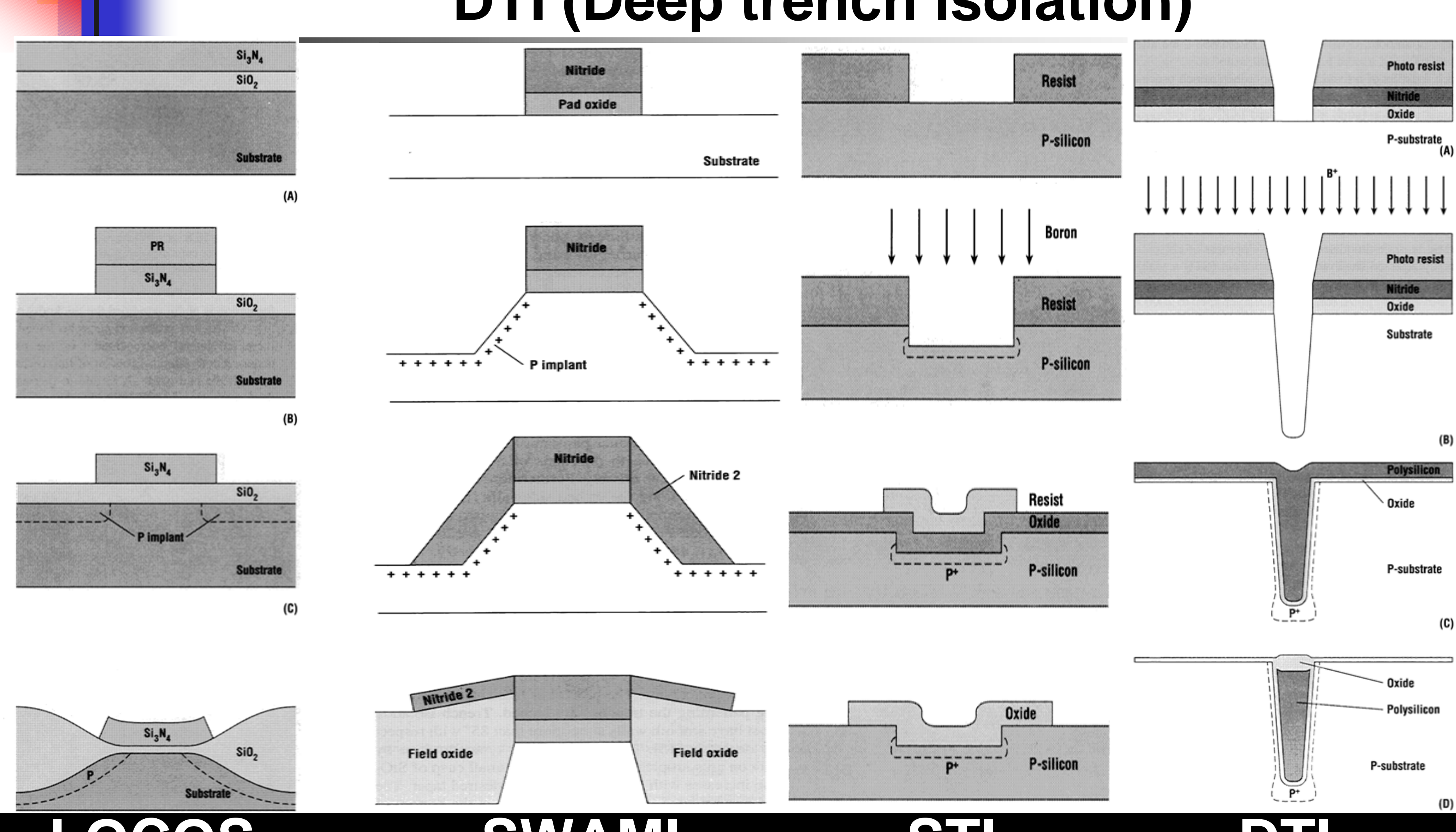
Insulating Barrier between Metal Layers

Purpose: Serves as protective layer between metals.
Common film thickness : 5000 ~10000 Å

Comments: This oxide is not thermally grown, but is deposited.

Interlayer Dielectric (oxide)
Passivation layer
Bonding pad metal
ILD-5
M-4
ILD-4
M-3

LOCOS (Local oxidation of silicon) SWAMI (Sidewall masked isolation) STI (Shallow trench isolation) DTI (Deep trench isolation)

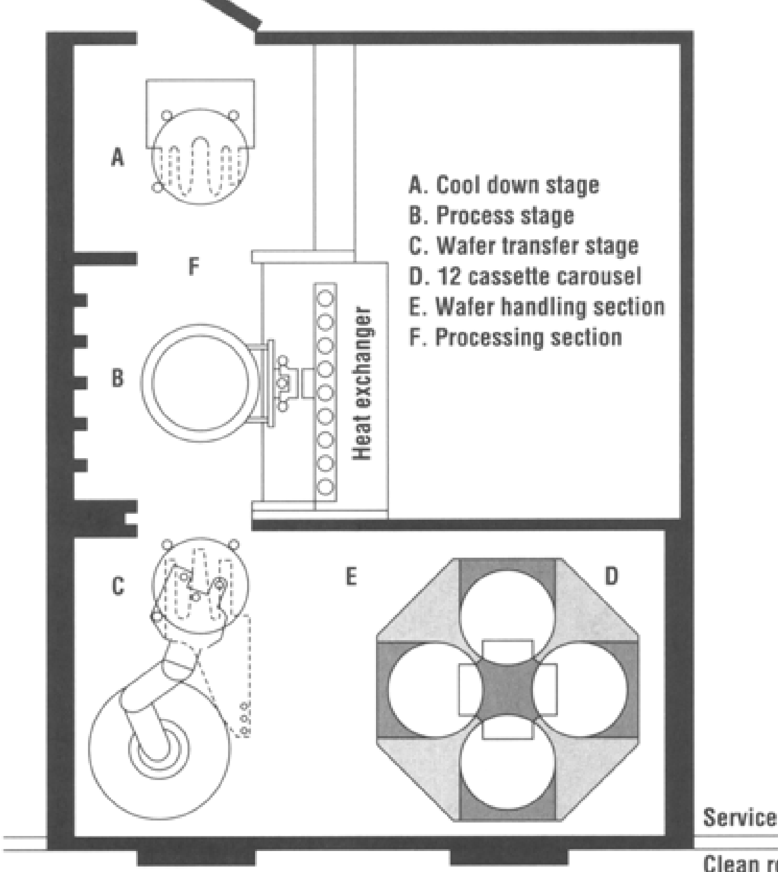


Thermal Oxidation Furnace

Horizontal Oxidation/Diffusion Furnace

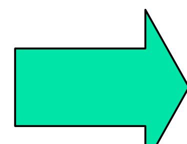
Vertical Oxidation/Diffusion Furnace

Photograph courtesy of International SEMATECH



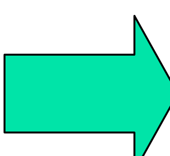
Thermal Oxidation Process Flow Chart

- Chemicals
- % solution
- Temperature
- Time



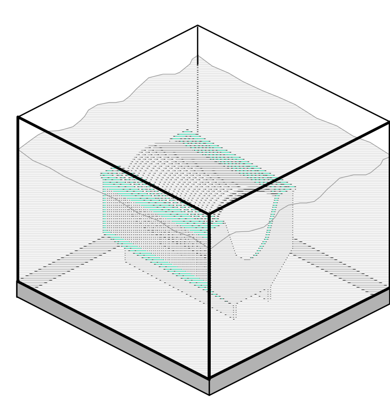
Oxidation Furnace

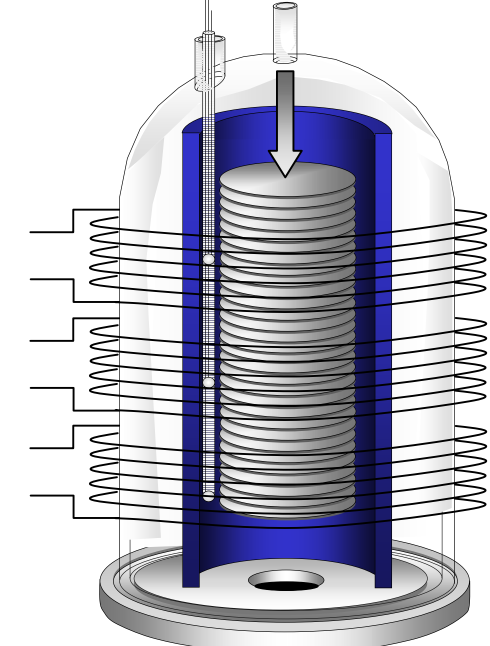
- O_2, H_2 , N_2 , Cl
- Flow rate
- Exhaust
- Temperature
- Temperature profile
- Time

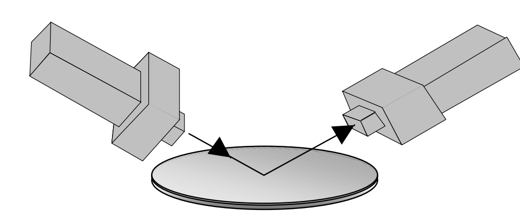


Inspection

- Film thickness
- Uniformity
- Particles
- Defects





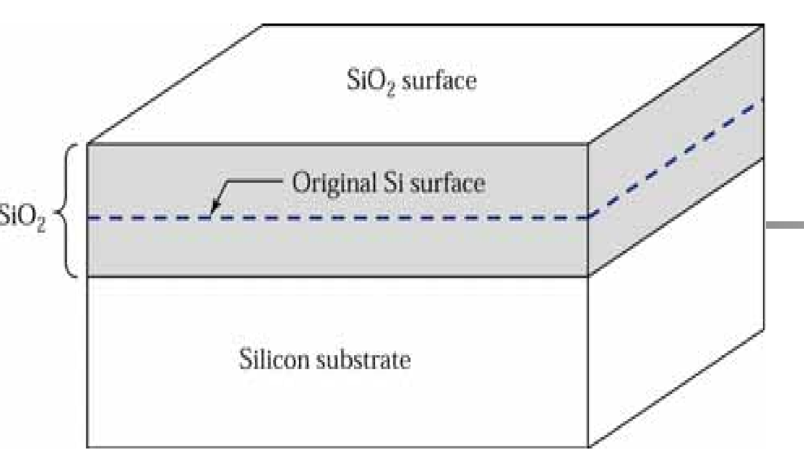


Process Recipe for Dry Oxidation Process

Step	Time (min)	Temp (ºC)	N_2 Purge Gas (slm)	Process Gas N_2 (slm)	Process Gas O_2 (slm)	Process Gas HCl (sccm)	Comments
0		850	8.0	0	0	0	Idle condition
1	5	850		8.0	0	0	Load furnace tube
2	7.5	Ramp 20ºC/min		8.0	0	0	Ramp temperature up
3	5	1000		8.0	0	0	Temperature stabilization
4	30	1000		0	2.5	67	Dry oxidation
5	30	1000		8.0	0	0	Anneal
6	30	Ramp -5ºC/min		8.0	0	0	Ramp temperature down
7	5	850		8.0	0	0	Unload furnace tube
8		850	8.0	0	0	0	Idle

Note: gas flow units are slm (standard liters per minute) and sccm (standard cubic centimeters per minute)

Kinetics of Oxidation



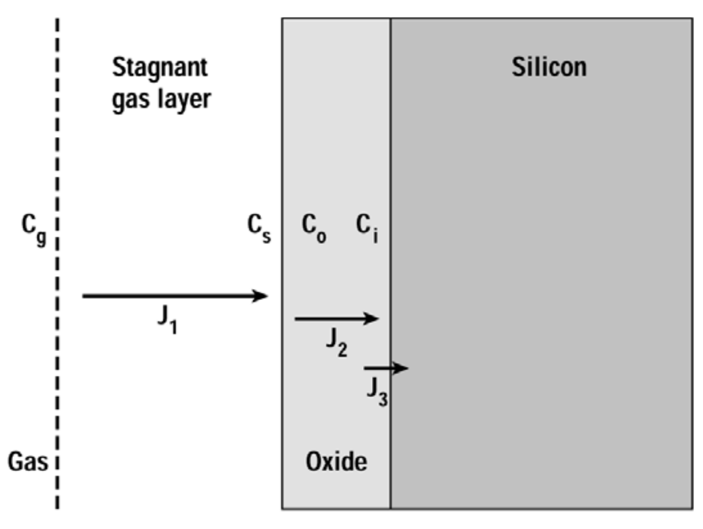
Growth of SiO_2 by thermal oxidation.

- During Oxidation, the oxidizing species
  - Step1: must transport from gas bulk to gas- oxide interface.
  - Step2: must diffusion across the existing oxide layer.
  - Step3: must react at the silicon surface.

Dry oxidation: $Si + O_2 \rightarrow SiO_2$

Wet oxidation: $Si + H_2O \rightarrow SiO_2 + 2H_2$

g:gas, s:surface, o:oxide, i:interface



Schematic diagram of the oxidation flows

$$\text{Fick's 1st law}: J_1 \approx D_{O_2} \frac{C_g - C_s}{t_{sl}} = J_{gas} = h_g (C_g - C_s)$$

h_g : mass transport coefficient ; C : oxygen concentration

$$J_2 \approx D_{O_2} \frac{C_o - C_i}{t_{ox}} \quad ; \quad J_3 = k_s C_i \quad (k_s : \text{chemical rate constant})$$

$$\text{Steady state}: J_1 = J_2 = J_3$$

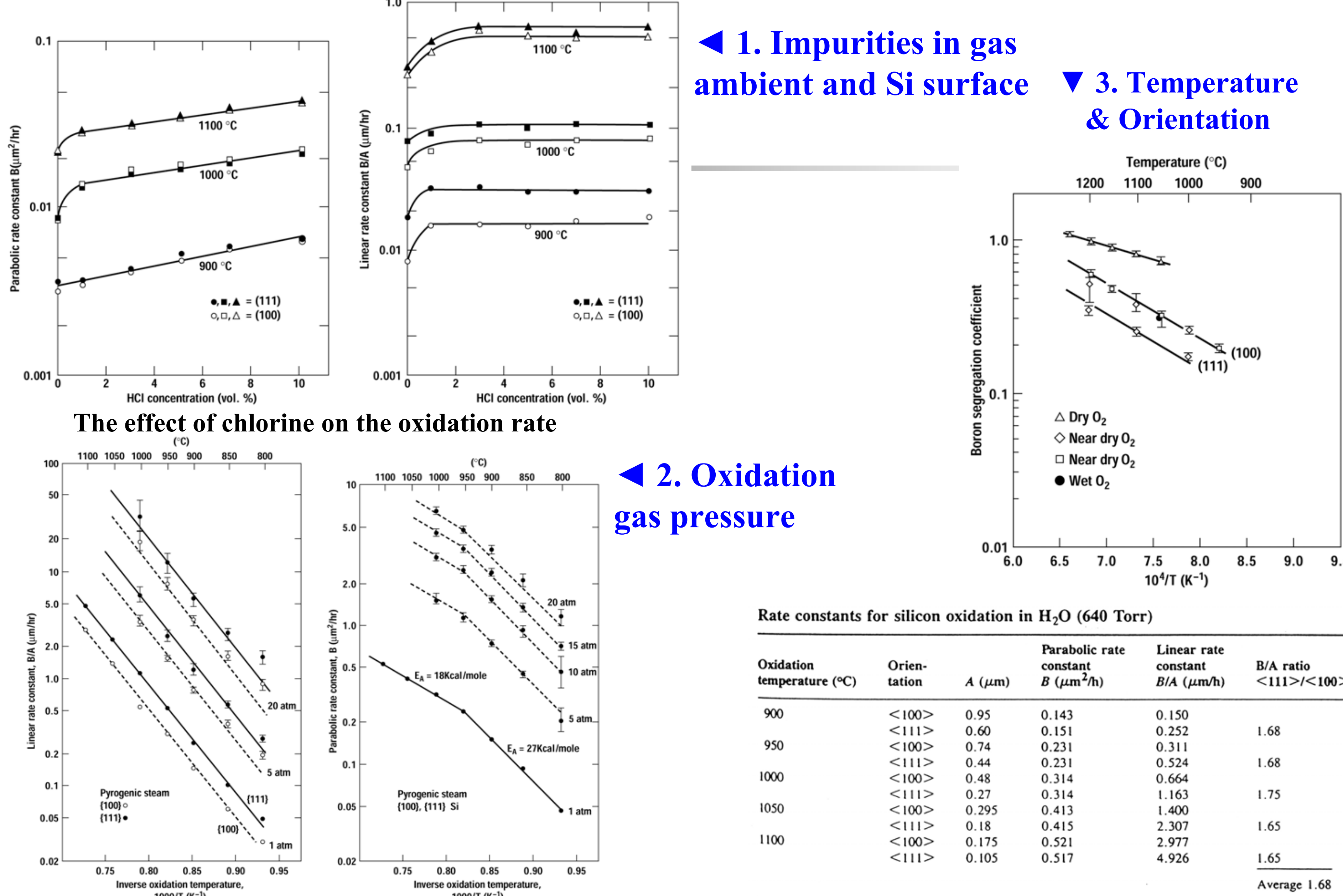
$$\Rightarrow t_{ox}^2 + A t_{ox} = B(t + \tau)$$

$$when\ (t + \tau) << A^2 / 4B \Rightarrow t_{ox} \approx \frac{B}{A}(t + \tau): linear\ law$$

$$when\ t >> \tau;\ A^2 / 4B \Rightarrow t_{ox}^2 \approx B(t + \tau): parabolic\ law$$

(B/A : linear rate coeff. ; B : parabolic rate coeff.)

Factors Influence Oxidation Rates



The effect of chlorine on the oxidation rate

Rate constants for silicon oxidation in H_2O (640 Torr)

Oxidation temperature (°C)	Orientation	A (μm)	Parabolic rate constant B (μm^2/h)	Linear rate constant B/A (μm/h)	B/A ratio <111>/<100>
900	<100>	0.95	0.143	0.150	
	<111>	0.60	0.151	0.252	1.68
950	<100>	0.74	0.231	0.311	
	<111>	0.44	0.231	0.524	1.68
1000	<100>	0.48	0.314	0.664	
	<111>	0.27	0.314	1.163	1.75
1050	<100>	0.295	0.413	1.400	
	<111>	0.18	0.415	2.307	1.65
1100	<100>	0.175	0.521	2.977	
	<111>	0.105	0.517	4.926	1.65
					Average 1.68

High pressure studies of the parabolic and linear rate coefficients in steam

Factors Influence Oxidation Rates

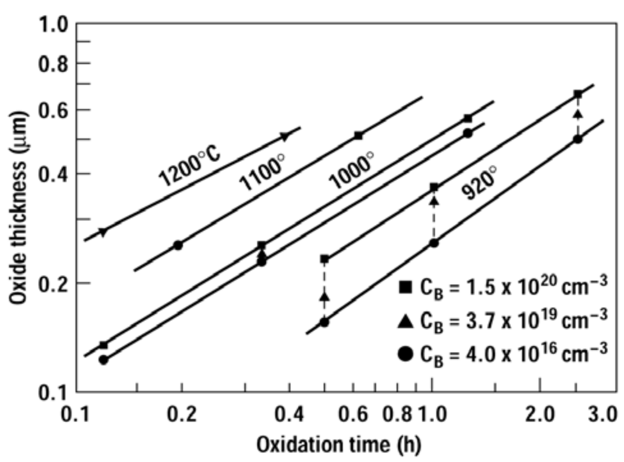


Figure 4.18 Silicon dioxide thickness versus wet oxidation time for three different surface concentrations of boron *(after Deal et al., reprinted by permission, The Electrochemical Society).*

◀ **4. Time & Substrate Doping**

▼ **5. Oxidant Species**

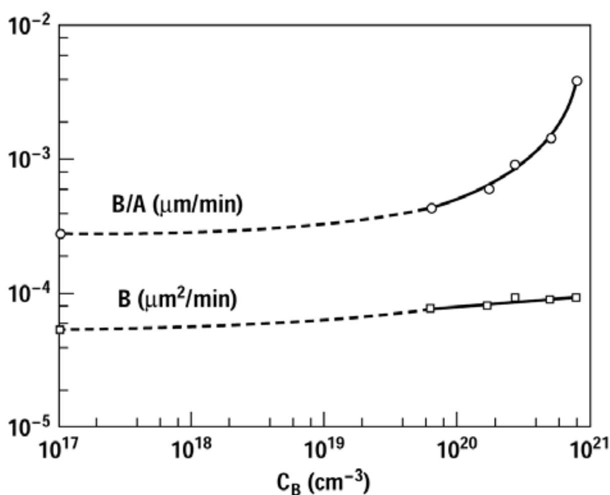
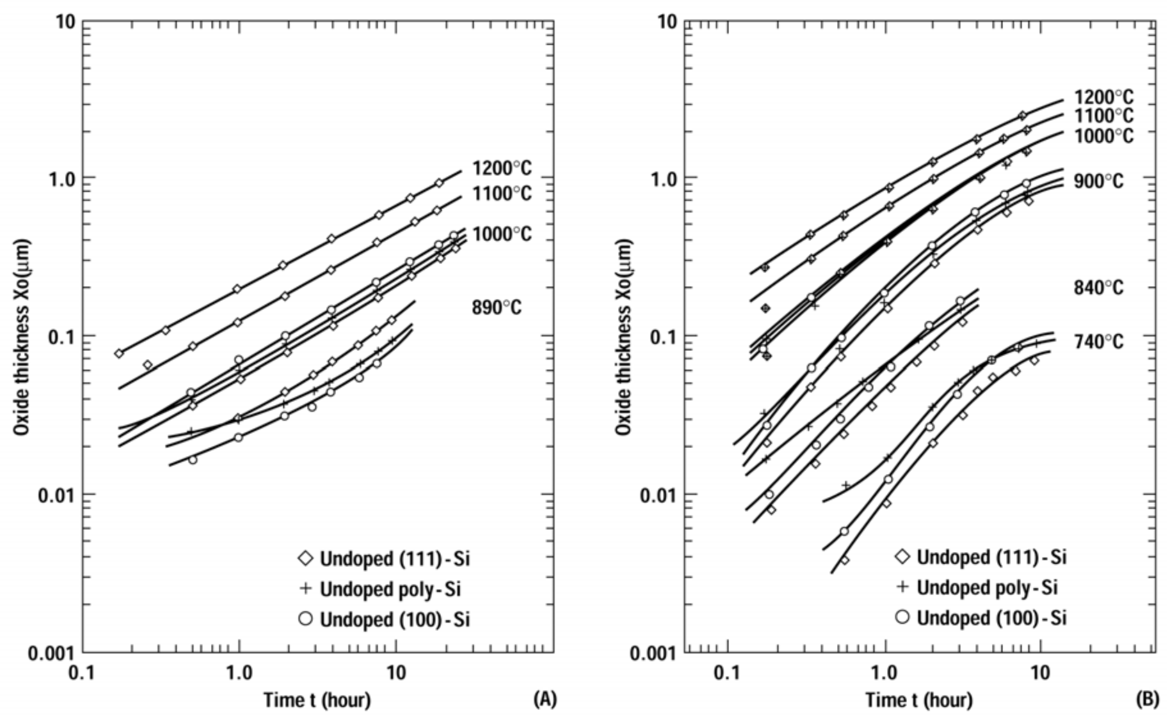
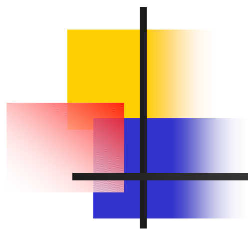


Figure 4.19 Oxidation rate coefficients for dry oxygen at 9007C as functions of the surface concentration of phosphorus *(after Ho et al., reprinted by permission, The Electrochemical Society).*



The oxidation of undoped polysilicon in (A) wet and (B) dry ambients.

Color Chart for Thermal Grown SiO_2 Films



- **Film Thickness**
  - **Ellipsometry** (Transparent Films)
  - **Nanospec**: interference
  - Reflection Spectroscopy
  - X-ray Film Thickness
  - Photoacoustic Technology
- **Resistivity and Sheet Resistance**
  - **Four-Point Probe**

Film Thickness (μm)	Color and Comments	Film Thickness (μm)	Color and Comments
0.05	Tan	0.54	Yellow green
0.07	Brown	0.56	Green yellow
0.10	Dark violet to red violet	0.57	Yellow to "yellowish" (not yellow but is in the position where yellow is to be expected; at times appears to be light creamy gray or metallic)
0.12	Royal blue		
0.15	Light blue to metallic blue		
0.17	Metallic to very light yellow green		
0.20	Light gold or yellow; slightly metallic	0.58	Light orange or yellow to pink borderline
0.22	Gold with slight yellow orange	0.60	Carnation pink
		0.63	Violet red
0.25	Orange to melon	0.68	"Bluish" (not blue but borderline between violet and blue green; appears more like a mixture between violet red and blue green and looks grayish)
0.27	Red violet		
0.30	Blue to violet blue		
0.31	Blue		
0.32	Blue to blue green		
0.34	Light green	0.72	Blue green to green (quite broad)
0.35	Green to yellow green		
0.36	Yellow green	0.77	"Yellowish"
0.37	Green yellow	0.80	Orange (rather broad for orange)
0.39	Yellow	0.82	Salmon
0.41	Light orange	0.85	Dull, light red violet
0.42	Carnation pink	0.86	Violet
0.44	Violet red	0.87	Blue violet
0.46	Red violet	0.89	Blue
0.47	Violet	0.92	Blue green
0.48	Blue violet	0.95	Dull yellow green
0.49	Blue	0.97	Yellow to "yellowish"
0.50	Blue green	0.99	Orange
0.52	Green (broad)	1.00	Carnation pink

Oxide Charges

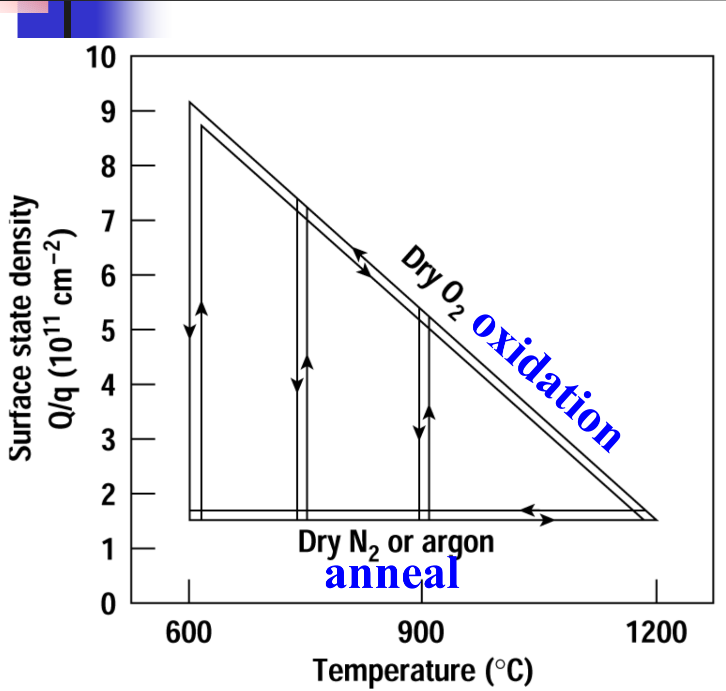


Figure 4.12 The Deal triangle showing the effects of a high-temperature inert (nitrogen or argon) postoxidation anneal on interface states and fixed charge density *(after Deal et al., reprinted by permission, The Electrochemical Society).*

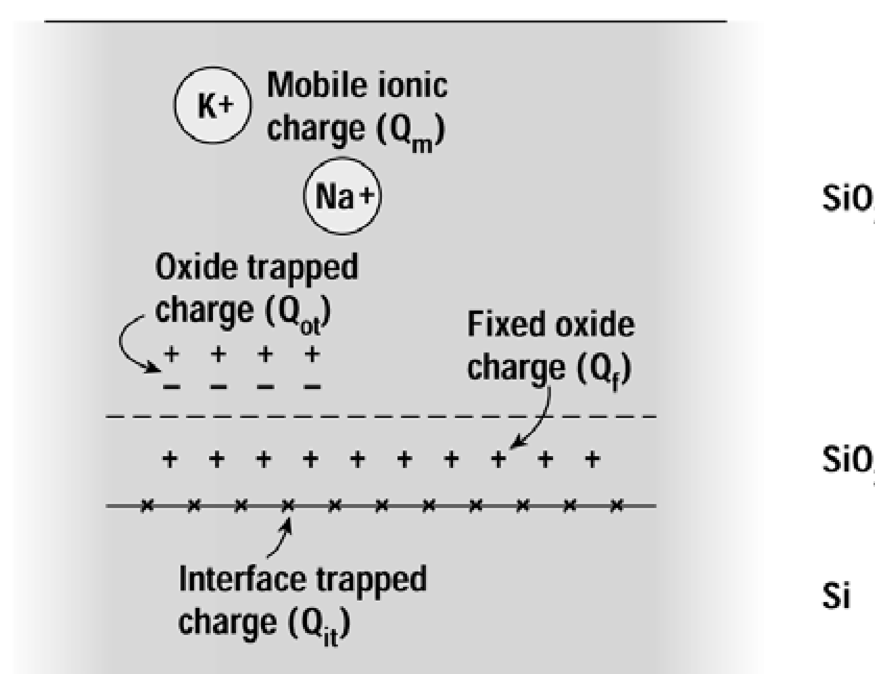
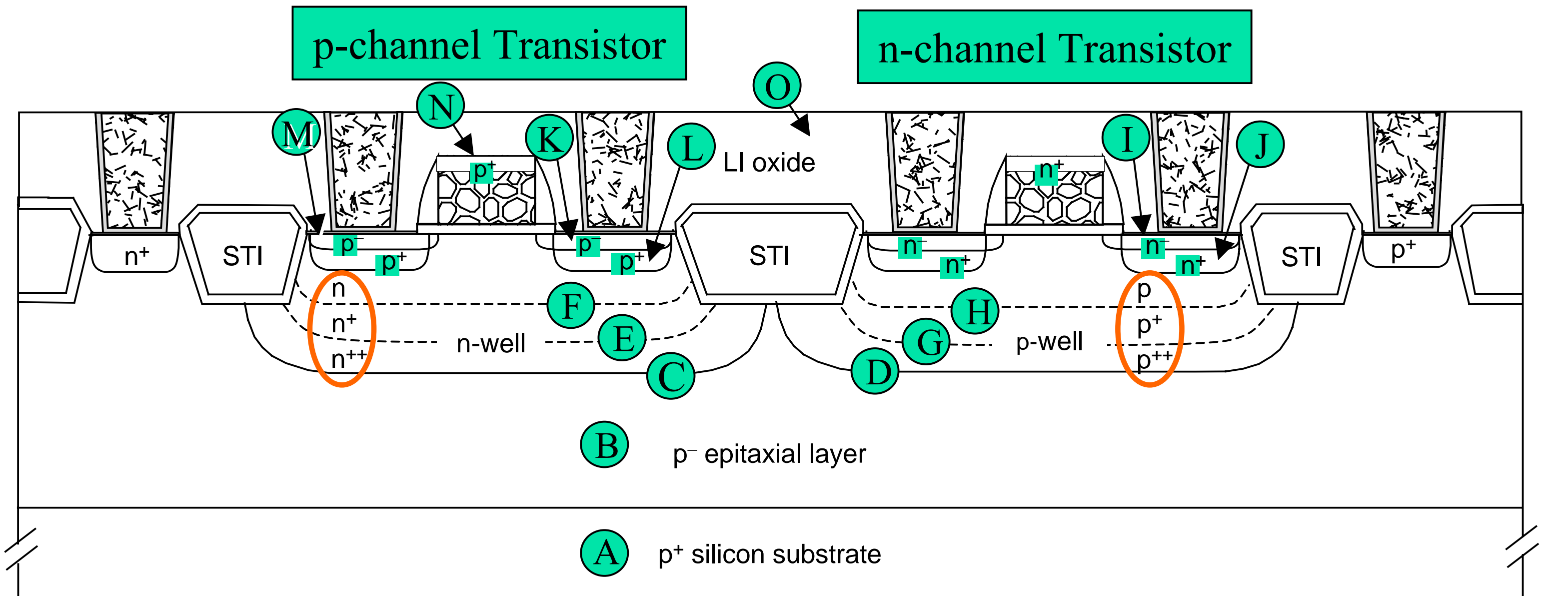


Figure 4.14 Silicon–silicon dioxide structure with mobile, fixed charge, and interface states *(© 1980, IEEE, after Deal).*

Diffusion & Ion Implant Applications

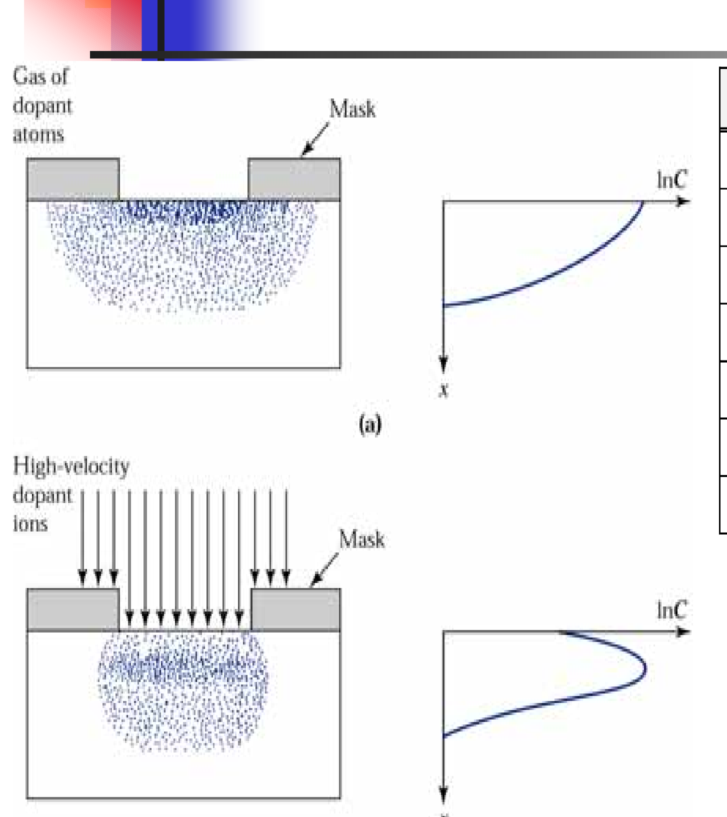
Process Step	Dopant	Method
A. p+ Silicon Substrate	B	Diffusion
B. p^- Epitaxial Layer	B	Diffusion
C. Retrograde n-Well	P	Ion Implant
D. Retrograde p-well	B	Ion Implant
E. p-Channel Punchthrough	P	Ion Implant
F. p-Channel Threshold Voltage (V_T) Adjust	P	Ion Implant
G. np-Channel Punchthrough	B	Ion Implant
H. np-Channel V_T Adjust	B	Ion Implant

I. n-Channel Lightly Doped Drain (LDD)	As	Ion Implant
J. n-Channel Source/Drain (S/D)	As	Ion Implant
K. p-Channel LDD	BF_2	Ion Implant
L. p-Channel S/D	BF_2	Ion Implant
M. Silicon	Si	Ion Implant
N. Doped Polysilicon	P or B	Ion Implant or Diffusion
O. Doped SiO_2	P or B	Ion Implant or Diffusion



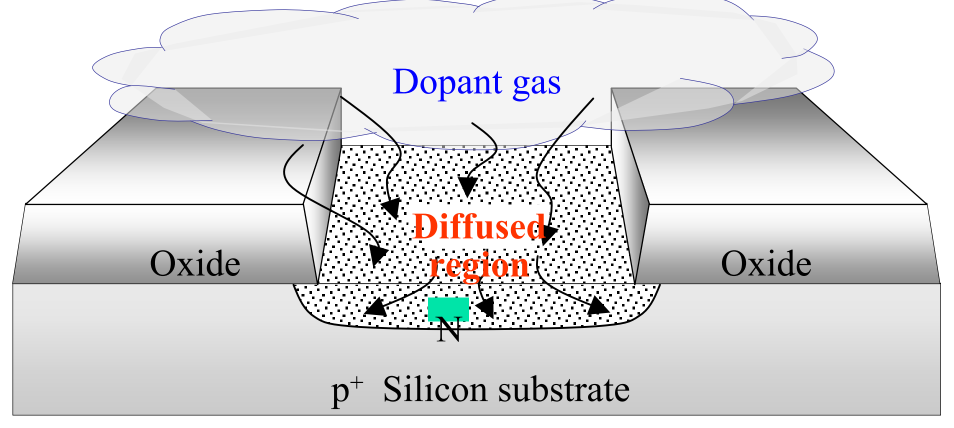
Common Dopant Processes in CMOS Fabrication

Impurity Doping - Diffusion



Dopant	Formula of Source	Chemical Name
Arsenic (As)	AsH_3	Arsine (gas)
Phosphorus (P)	PH_3	Phosphine (gas)
Phosphorus (P)	$POCl_3$	Phosphorus oxychloride (liquid)
Boron (B)	B_2H_6	Diborane (gas)
Boron (B)	BF_3	Boron tri-fluoride (gas)
Boron (B)	BBr_3	Boron tri-bromide (liquid)
Antimony (Sb)	$SbCl_5$	Antimony pentachloride (solid)

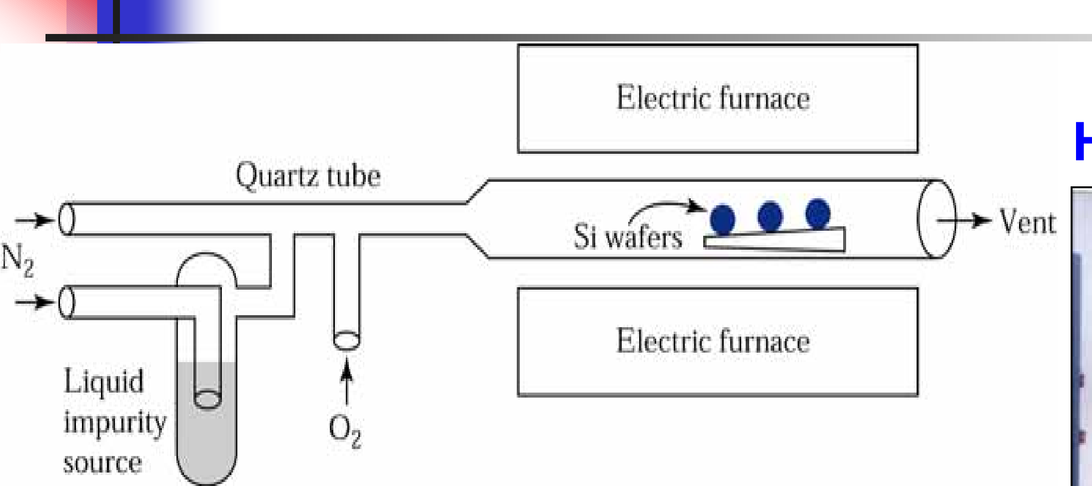
Typical Dopant Sources for Diffusion



Comparison of (*a*) diffusion and (*b*) ion-implantation techniques for the selective introduction of dopants into the semiconductor substrate.

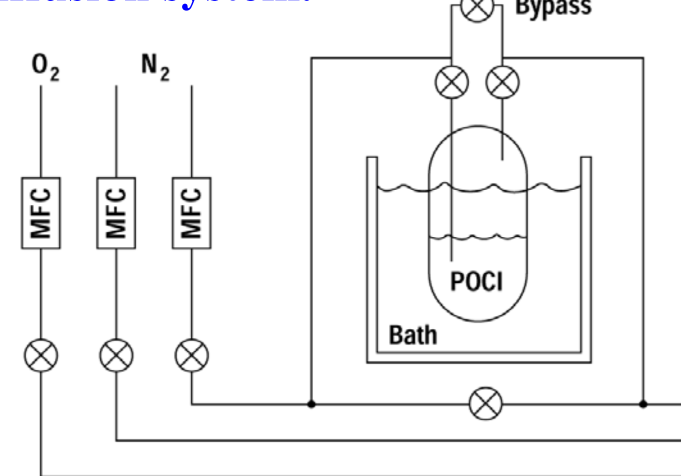
Doped Region in a Silicon Wafer

Diffusion Facility



The schematic diagram of a typical open-tube diffusion system.

Horizontal Diffusion Furnace

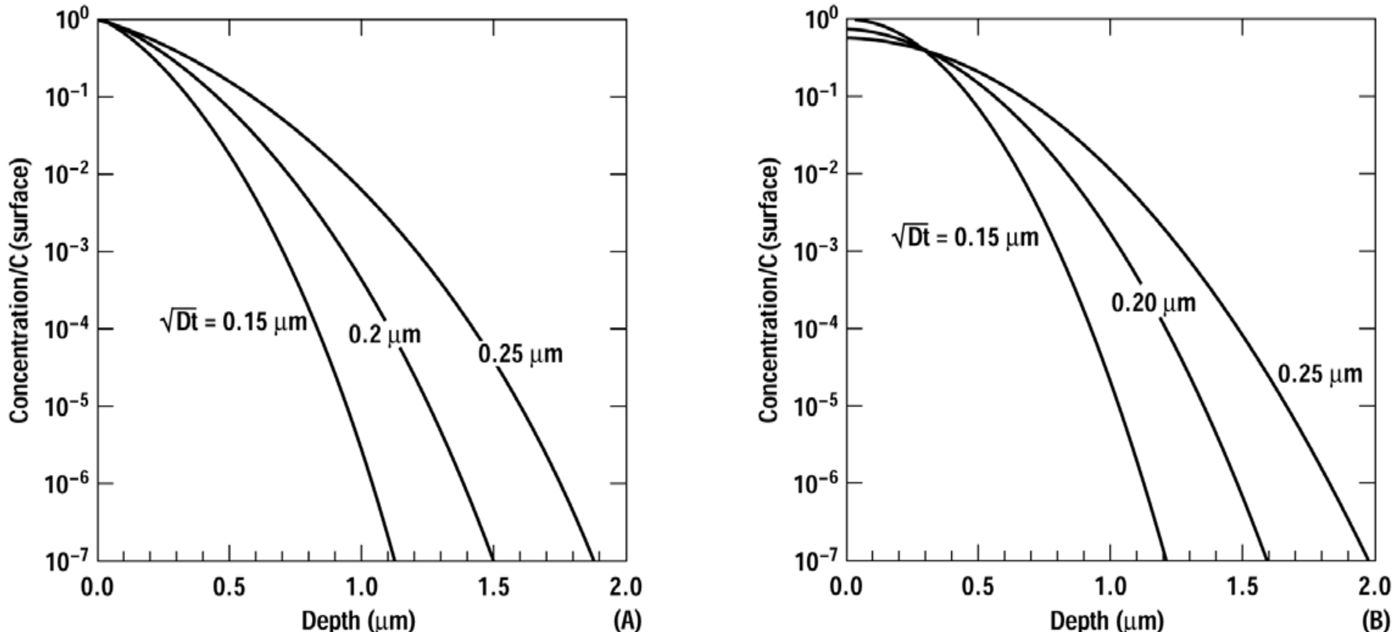


A typical bubbler arrangement for doping a silicon wafer using a POCL source. The gas flow is set using mass flow controllers (MFC).

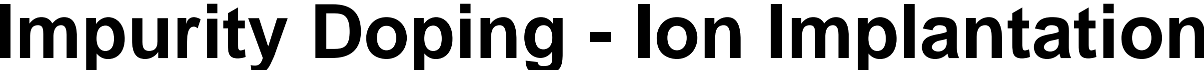
Diffusion Process

Six Steps for Successful Diffusion:

1. Download the process recipe with the desired diffusion parameters.
2. Set up the furnace, including a temperature profile.
3. Clean the wafers and dip in HF to remove native oxide.
4. Perform predeposition: load wafers into the deposition furnace and diffuse the dopant.
5. Perform drive-in: increase temperature to drive-in and activate the dopant bonds, then unload the wafers.
6. Measure, evaluate and record junction depth and sheet resistivity.

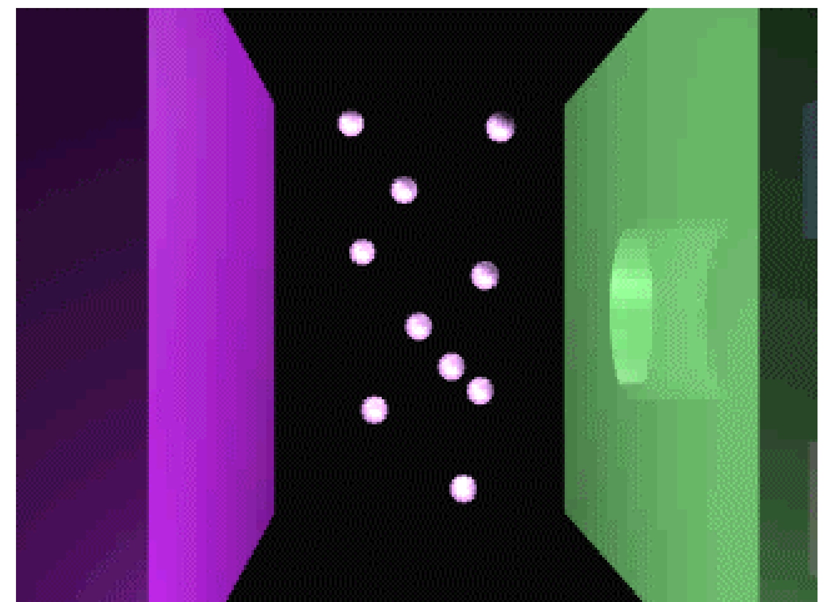


Concentration as a function of depth for (A) predeposition and (B) drive in diffusion for several values of the characteristic diffusion length.



Impurity Doping - Ion Implantation

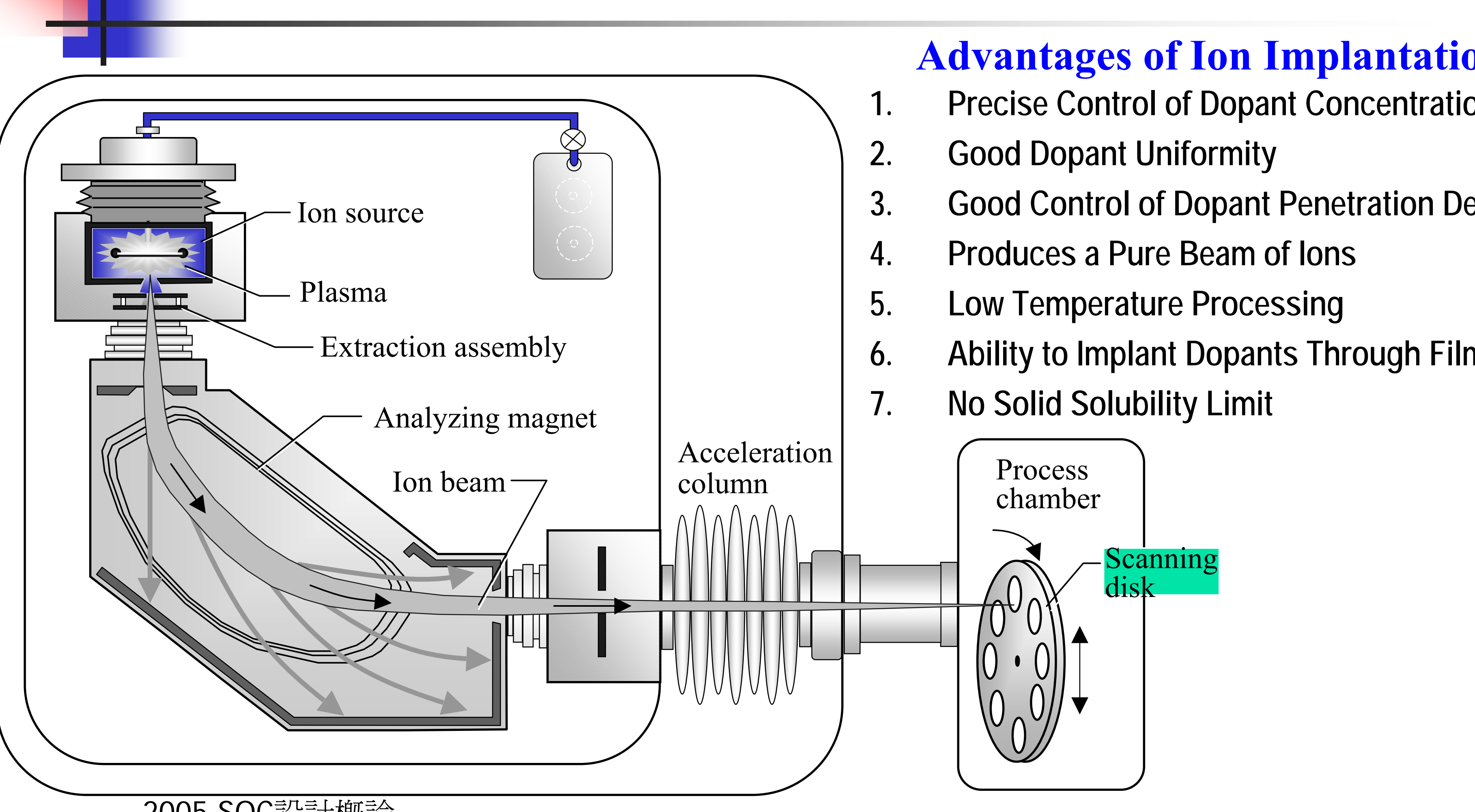
- **Introduce Impurities (Dopants)**
  - **To change the electrical properties of the silicon**
  - **The most common method for introducing impurities into silicon wafers**
    - **Impurities with an electric charge are accelerated to high energy and shot into the exposed area of the wafer surface**



Impurity Doping – Ion Implantation

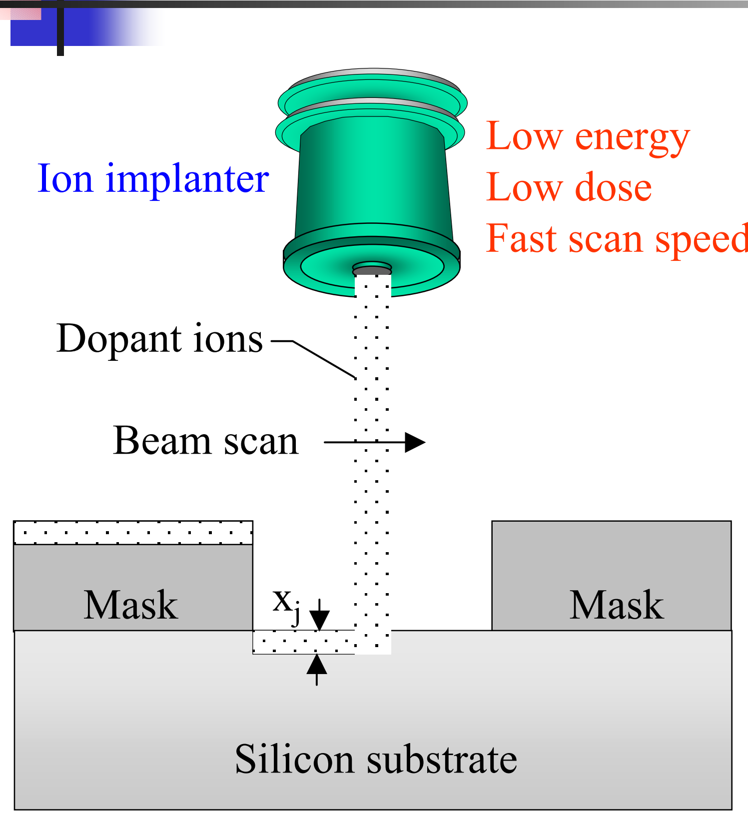
Advantages of Ion Implantation

1. Precise Control of Dopant Concentration
2. Good Dopant Uniformity
3. Good Control of Dopant Penetration Depth
4. Produces a Pure Beam of Ions
5. Low Temperature Processing
6. Ability to Implant Dopants Through Films
7. No Solid Solubility Limit

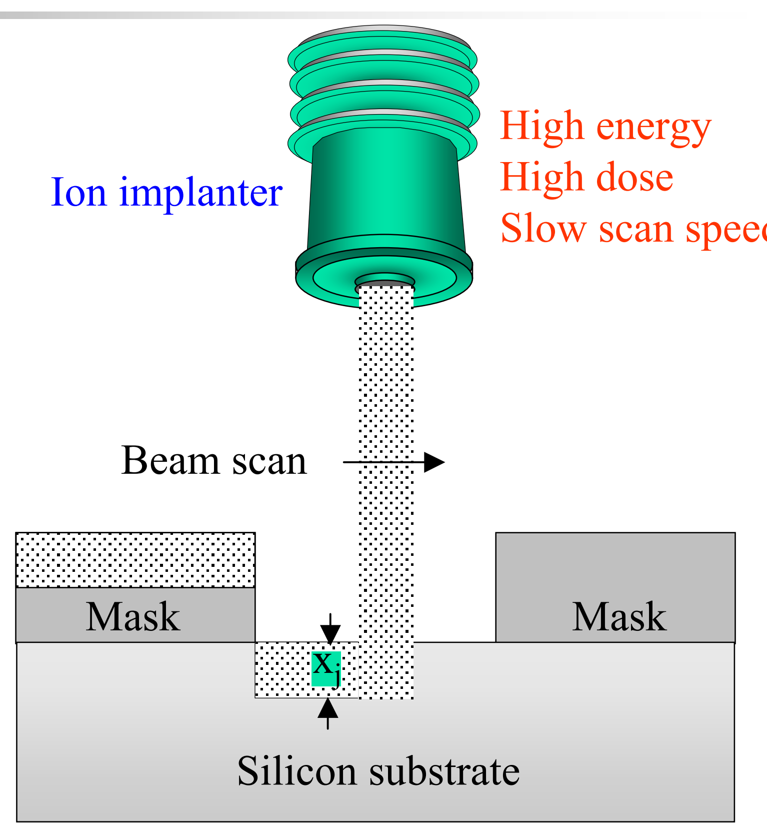


Impurity Doping – Ion Implantation

Controlling Dopant Concentration and Depth



a) Low dopant concentration (n^-, p^-) and shallow junction (x_j)



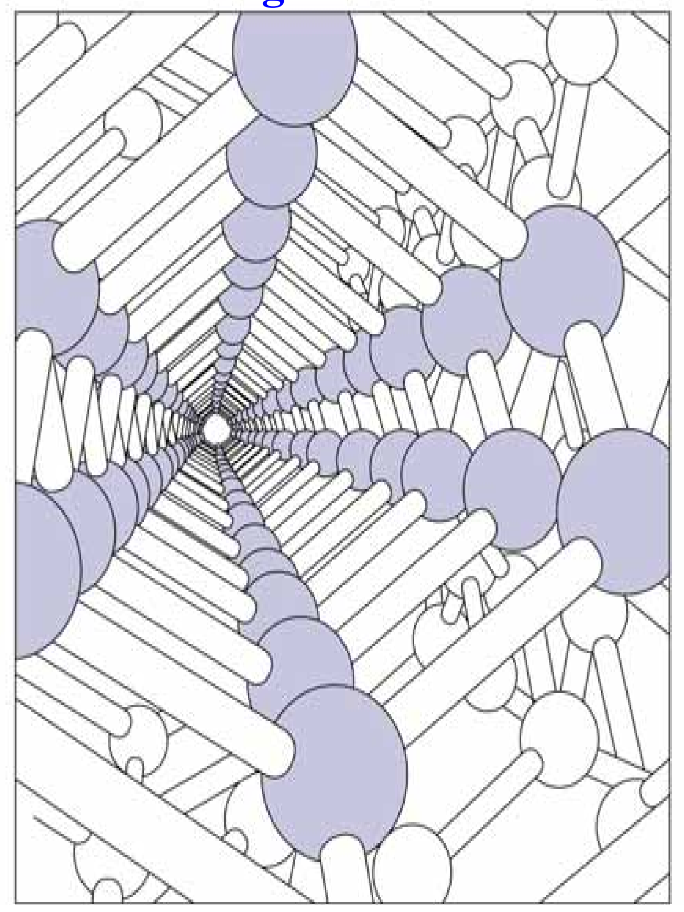
b) High dopant concentration (n^+, p^+) and deep junction (x_j)

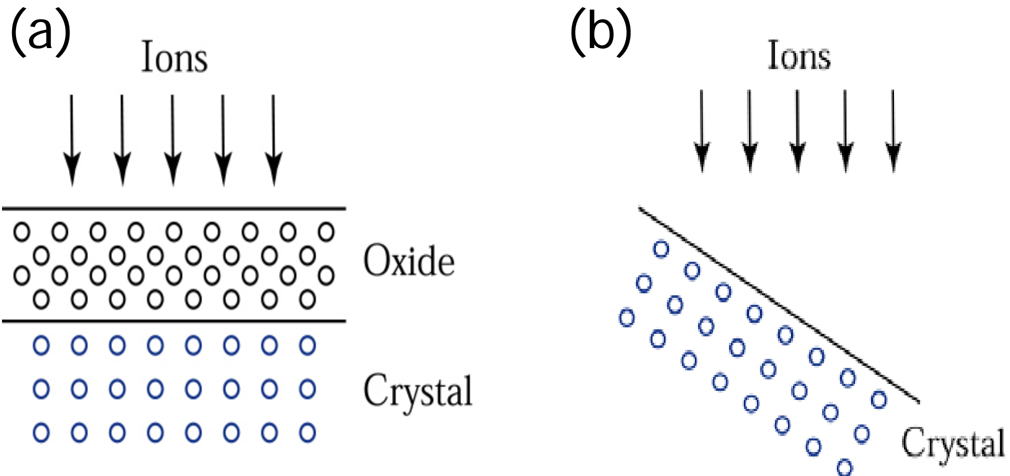
Classes of Implanters

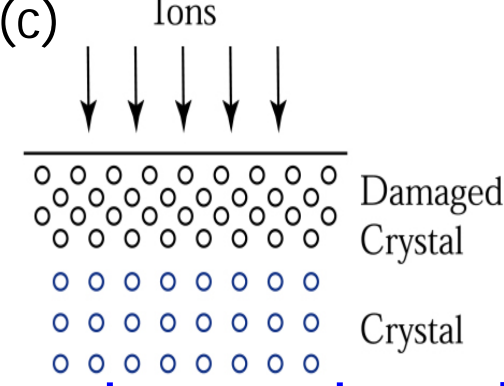
Class of Implanter System	Description and Applications
Medium Current	• Highly pure beam currents <10 mA. • Beam energy is usually < 180 keV. • Most often the ion beam is stationary and the wafer is scanned. • Specialized applications of punchthrough stops.
High Current	• Generate beam currents > 10 mA and up to 25 mA for high dose implants. • Beam energy is usually <120 keV. • Most often the wafer is stationary and the ion beam does the scanning. • Ultralow-energy beams (<4keV down to 200 eV) for implanting ultrashallow source/drain junctions.
High Energy	• Beam energy exceeds 200 keV up to several MeV. • Place dopants beneath a trench or thick oxide layer. • Able to form retrograde wells and buried layers.
Oxygen Ion Implanters	• Class of high current systems used to implant oxygen in silicon-on-insulator (SOI) applications.

Ion Channeling

Model for a diamond structure, viewed along a <110> axis.



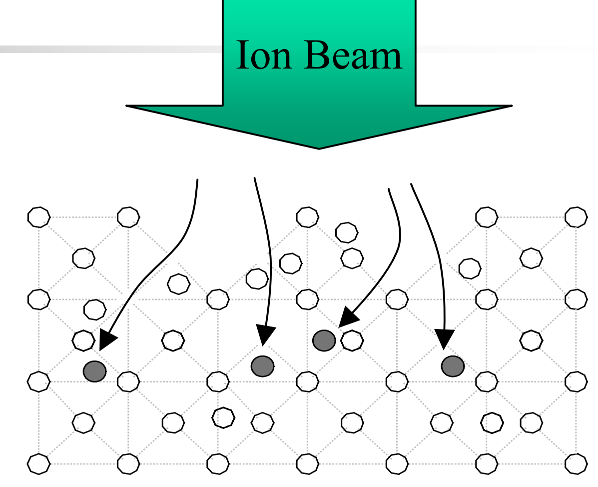




(a) implant through an amorphous oxide layer,
(b) misorient the beam direction to all crystal axes
(c) predamage on the crystal surface.

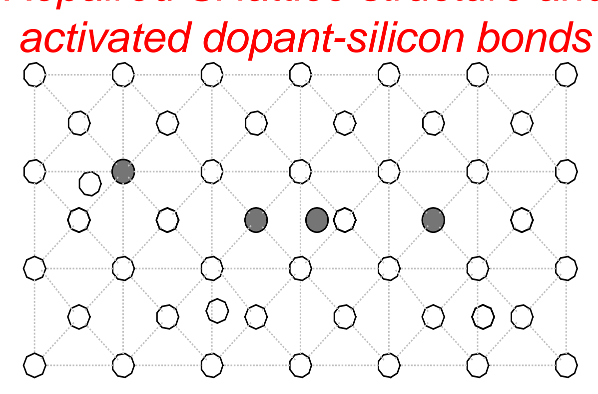
Implant Damage & Annealing

Implantation disorder caused by (*a*) light ions and (*b*) heavy ions.



a) Damaged Si lattice during implant

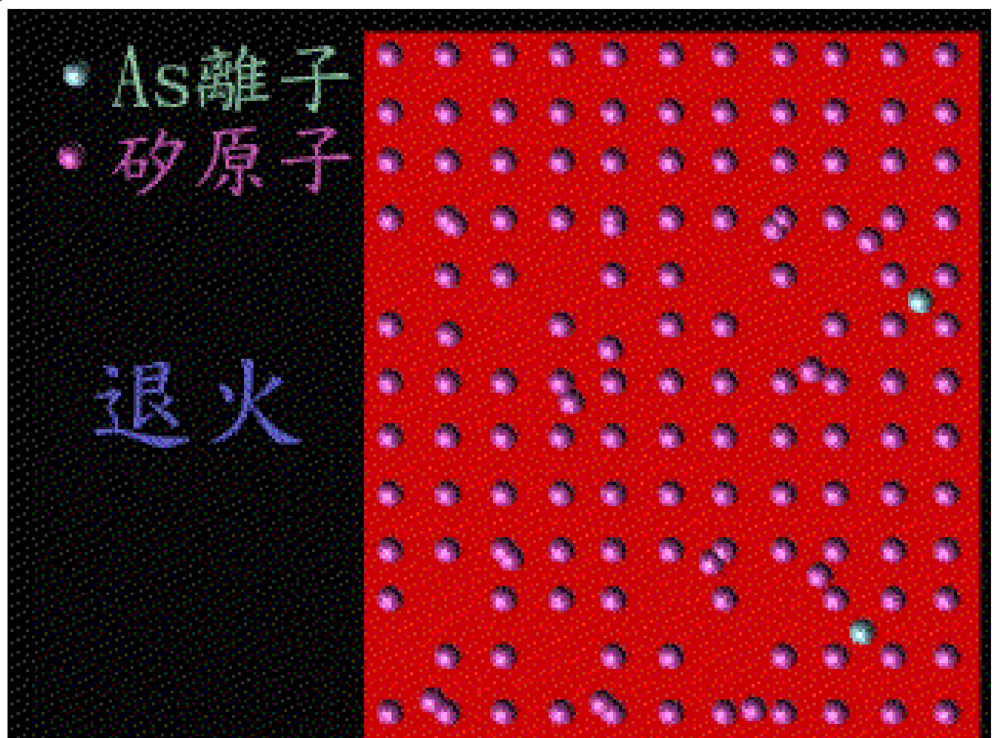
Repaired Si lattice structure and activated dopant-silicon bonds



b) Si lattice after annealing

Ion Implementation

- **Annealing**
  - **Following the ion implementation**
    - **A high temperature furnace process is used to anneal out the damage**



Analysis of Diffused Profiles

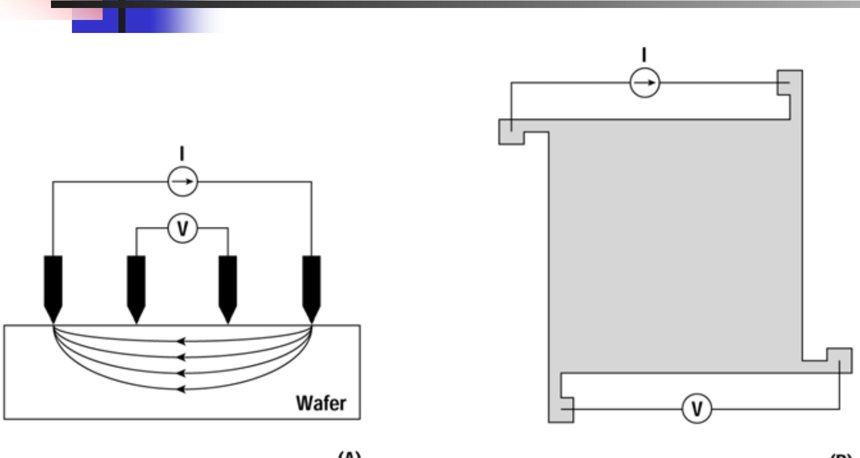


Figure 3.14 The four point probe (A) and Van der Pauw (B) methods for determining the resistivity of a sample.

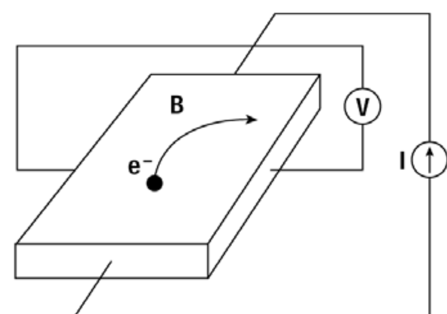


Figure 3.16 The Hall effect is able to simultaneously measure the carrier type, mobility, and sheet concentration.

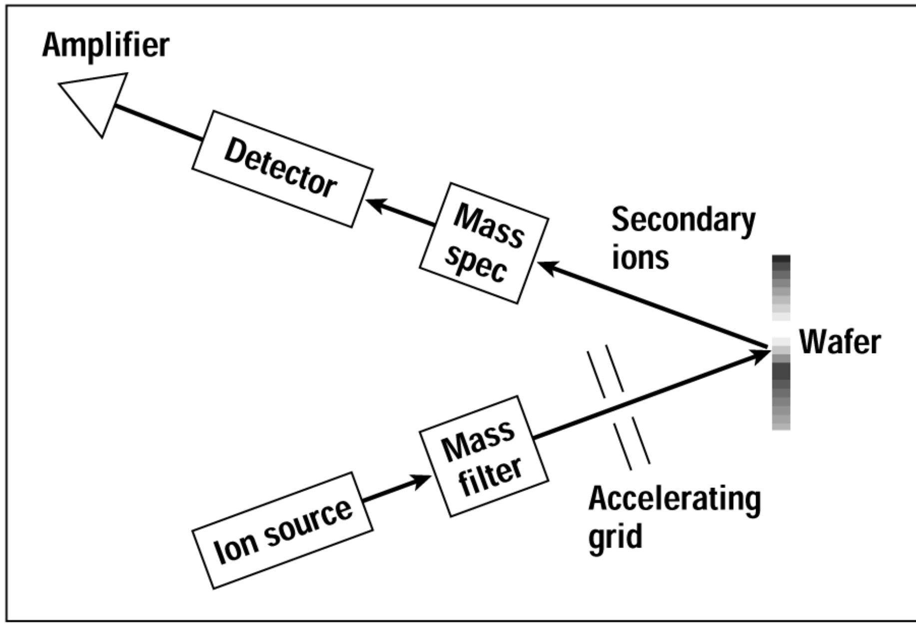


Figure 3.18 A typical SIMS arrangement. The sample is bombarded by high-energy ions. The sputtered material is mass analyzed to determine the composition of the substrate.