Low Power FSK Receiver Using an Oscillator-Based Injection-Locked Frequency Divider

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***Abstract*—This letter presents a novel frequency-shift keying (FSK) receiver using an oscillator-based injection-locked frequency divider (ILFD), thereby achieving high sensitivity, low dc-offset, and low power consumption. The proposed receiver comprises a low-noise amplifier, a divide-by-2 ring-oscillator-based ILFD, and a subharmonic mixer. Moreover, the proposed receiver is fabricated using 0.18 μm CMOS process and consumes 1.1 mW. Measurement results demonstrate that the proposed receiver has a sensitivity of -83 dBm at 10^{-3} bit error rate with 1 Mb/s data rate in receiving a 2.4 GHz Gaussian FSK signal.**

***Index Terms*—CMOS FSK receiver, injection-locked frequency divider (ILFD), ring oscillator, subharmonic mixer.**

I. Introduction

INJECTION-locked oscillators (ILOs) are widely used in frequency-shift keying (FSK) RF receivers [1]–[4]. Given the ability to remove a power-hungry phase-locked-loop (PLL)-based carrier recovery circuitry, the ILO-based FSK receivers are feasible for low power and data rate applications, including wireless sensor networks (WSNs) and wireless body area networks (WBANs). However, despite their potential for low power consumption, these receivers generally incur an insufficient sensitivity due to a limited locking range at low input power levels [2], [3]. In [4], the use of a trifilar transformer splitter in an LC-ILO-based FSK receiver can significantly improve sensitivity. However, this design consumes large chip area and power consumption and causes a high dc offset.

This letter presents a novel 2.4 GHz injection-locked-frequency-divider (ILFD)-based FSK receiver, consisting of a low noise amplifier (LNA), a divide-by-2 ring-oscillator-based ILFD, and a subharmonic mixer (SHM). The ILFD can provide larger locking range and lower power consumption than an ILO, thus assisting the proposed receiver to operate with high sensitivity and low power consumption. Moreover, the baseband dc offset is substantially reduced, owing to the use of a SHM in the proposed receiver.

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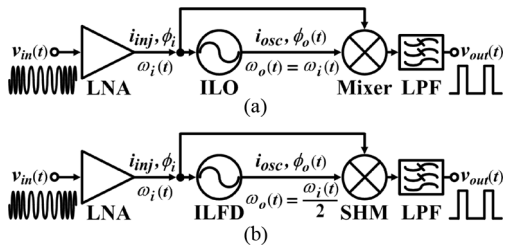

Fig. 1. Injection-locked FSK receiver architectures. (a) FSK receiver based on an ILO. (b) FSK receiver based on an oscillator-based ILFD.

II. ILFD-Based FSK Receiver Architecture

Fig. 1(a) shows a conventional ILO-based FSK receiver [3], [4]. Via an injection-locking process, the ILO and mixer perform an FM-to-PM and PM-to-AM conversion, respectively, to accomplish a noncoherent FSK demodulation. However, a dc offset induced by self-mixing in the mixer degrades the baseband signal quality and deteriorates the bit error rate (BER) performance. Moreover, since the ILO is the most power-consuming component in the system, the increasing ILO frequency leads to a larger power consumption of this receiver.

Fig. 1(b) shows the architecture of the proposed ILFD-based FSK receiver, in which $\omega_i(t)$ denotes the frequency of a received signal $v_{in}(t)$; $\omega_o(t)$ represents the free-running frequency of the oscillator required by the ILFD; i_{inj} and i_{osc} stand for the injection and oscillation current, respectively; and ϕ_i and $\phi_o(t)$ refer to the phase of i_{inj} and i_{osc}, respectively. The comparison with Fig. 1(a) indicates that a divide-by-2 ILFD replaces the ILO in an ILO-based FSK receiver. Accordingly, the ILFD-based FSK receiver has lower power consumption than that of the ILO-based FSK receiver because the former uses an oscillator at half of the frequency of that required by the latter. Furthermore, besides its use in converting $\omega_o(t)$ into $2\omega_o(t)$, SHM acts as a phase detector to detect the phase difference between i_{inj} and i_{osc}. Importantly, since an SHM has a high LO-to-RF isolation, a dc offset caused by self-mixing is markedly decreased. Moreover, the proposed receiver architecture uses a ring-oscillator-based ILFD that can achieve larger locking range, lower power consumption and less chip area than a conventional LC-ILFD.

In the steady state of injection locking, the output voltage $v_{out}(t)$ of the proposed receiver is given by (1), in which k_c denotes the overall gain of the system; n represents the number of stages in the ring oscillator; and I_{Bias} stands for the biasing current of the ring oscillator [5]. Clearly, (1) indicates an FM-to-AM conversion

$$v_{out}(t) \approx \frac{k_c}{2}\left[\frac{n \cdot \sin\left(\frac{2\pi}{n}\right) \cdot I_{Bias}}{i_{inj}}\left(\frac{\omega_o(t) - \omega_i(t)/2}{\omega_o(t)}\right)\right]. \quad (1)$$

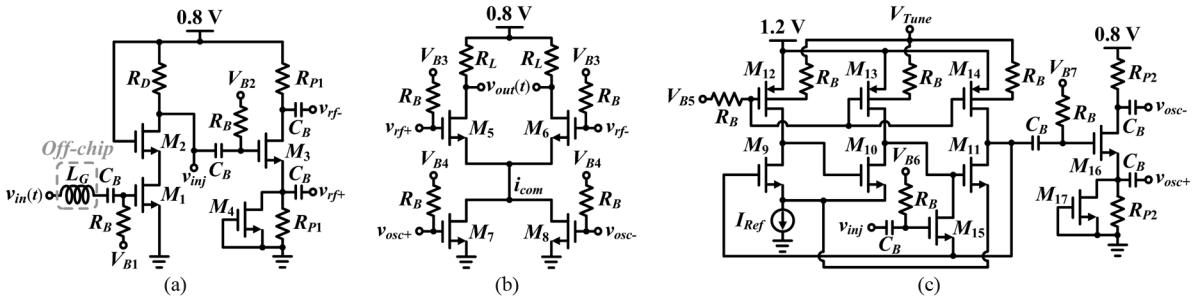

Fig. 2. Schematics of components in the proposed 2.4 GHz CMOS FSK receiver. (a) LNA with 0.55 mW power consumption. (b) SHM with 0.21 mW power consumption. (c) Divide-by-2 ring-oscillator-based ILFD with 0.34 mW power consumption.

To switch receiving channels, the ring oscillator frequency must be tuned close to the half frequencies of the receiving channels with an offset frequency less than the locking range.

III. Circuit Design

In order to further reduce power consumption and supply voltage of the proposed receiver, the sub-threshold and body-biasing techniques [6], [7] are applied to the LNA, active balun, and SHM of this receiver. Fig. 2(a) shows a cascode LNA with an output balun. The cascode LNA comprising transistors $M_{1,2}$ provides an input matching to the 50-Ω source impedance and amplifies the input signal $v_{in}(t)$, thus enhancing the sensitivity of the receiver. To make a good trade-off among noise figure (NF), gain, and linearity, transistors $M_{1,2}$ of 120-μm gate width, a resistor R_D of 600 Ω, and an external inductor L_G of 12 nH are used. Consequently, an NF of 2.5 dB and a voltage gain of 21 dB are achieved. The output balun is designed using a resistive loaded common-source amplifier with resistive degeneration. The gate width of transistor M_4 is chosen as twice the size of that of transistor M_3 to reduce the load impedance mismatch between the output differential terminals. Moreover, transistor M_3 with a gate width of 50 μm, transistor M_4 with a gate width of 100 μm, and resistor R_{P1} of 240 Ω are used in this balun to achieve amplitude and phase imbalance within 0.3 dB and 1.1°, respectively.

Fig. 2(b) shows a single-balanced SHM, in which the RF stage comprises transistors $M_{5,6}$, and the frequency doubler stage consists of transistors $M_{7,8}$. The common node current i_{com} at $2\omega_o(t)$ mixes with the RF stage current at $\omega_i(t)$. The mixing product current is converted into a differential voltage $v_{out}(t)$ via resistors R_L, in which $v_{out}(t)$ at $2\omega_o(t)$ is filtered out by an external low-pass filter. Transistors $M_{7,8}$ are biased near the threshold voltage to reduce the noise caused by non-ideal switching. Moreover, transistors $M_{5,6}$ with a gate width of 40 μm and transistors $M_{7,8}$ with a gate width of 35 μm are used in this SHM to attain a voltage gain of 15 dB and an NF of 12 dB.

An attempt is also made to reduce the power consumption of the proposed receiver by using a three-stage design of ring-oscillator-based ILFD [8]. Fig. 2(c) shows an ILFD with an output balun, in which the ILFD consists of transistors M_{9-11} with a gate width of 10 μm and transistors M_{12-14} with a gate width of 5 μm. Since the device size of transistor M_{15} influences the locking range of the ILFD, an optimum gate width of M_{15} is set at 10 μm. To avoid FM-to-PM distortion, M_{15} is biased near the weak inversion region to increase conversion loss while receiving an excessively high input voltage $v_{inj}(t)$. Moreover, to ensure that ILFD is stably locked in the tuning bandwidth by a received signal, the locking range of the ILFD is designed much larger than the frequency shift caused by the process, voltage and temperature (PVT) variations. Furthermore, a biasing circuit with temperature compensation is applied to ILFD for reducing frequency drift due to temperature variation. Notably, varying the body voltage V_{Tune} and biasing current I_{Ref} allows a maximum tuning range of 2.2 to 2.6 GHz for the ILFD. In the output balun, transistor M_{16} with a gate width of 40 μm, transistor M_{17} with a gate width of 80 μm, and resistor R_{P2} of 220 Ω are used to achieve an amplitude mismatch and phase error of less than 0.4 dB and 1.3°, respectively.

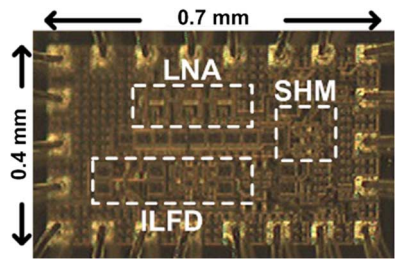

Fig. 3. Chip micrograph of the proposed ILFD-based FSK receiver.

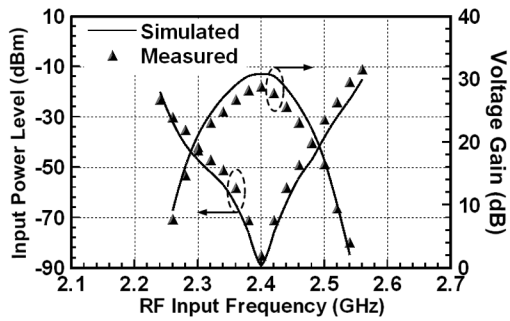

Fig. 4. Comparison of locking range and voltage gain between simulation and measurement for the proposed ILFD-based FSK receiver.

IV. Experimental Results

The proposed 2.4 GHz ILFD-based FSK receiver was fabricated using 0.18 μm CMOS technology. Fig. 3 shows a micrograph of the implemented chip, which occupies an area of 0.28 mm^2 including pads. A test buffer for ILFD is also integrated in this chip. An external operational amplifier was used during measurements, and the power dissipation P_{diss} of the chip alone is 1.1 mW. The measured input matching values of

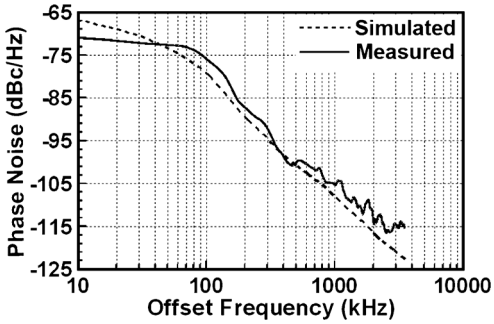

Fig. 5. Simulated and measured phase noise of the unlocked ILFD at 1.2 GHz.

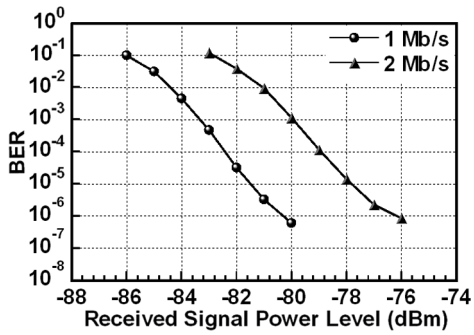

Fig. 6. Measured BER of the GFSK signals with different data rates.

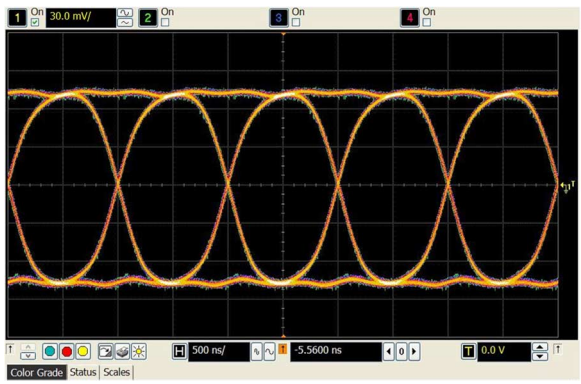

Fig. 7. Measured eye diagram of the demodulated GFSK signal at 1 Mb/s.

TABLE I
COMPARISON WITH PREVIOUS 2.4 GHZ GFSK RECEIVER DESIGNS

Reference	Sensitivity (dBm) @ 10^{-3} BER & 1 Mbps	Area (mm^2)	P_{diss} (mW)	CMOS (nm)
This work	-83 dBm	0.28	1.1[a]	180
[4]	-81 dBm	0.43	1.8[a]	90
[9]	-92 dBm	3	27.9[b]	130
[10]	-82.5 dBm	N/A	9.12[c]	180

[a] exclude external operation amplifier
[b] include variable gain LNA, demodulator, synthesizer, IF amplifier, ADC, and power management circuits
[c] include variable gain LNA, demodulator, synthesizer, and IF amplifier

the receiver are below −13 dB over 2.3–2.5 GHz. As a continuous-wave (CW) measurement result, Fig. 4 shows the input power level and voltage gain of the receiver operating in the boundary of the locking range. Measurement results indicate that the proposed receiver has a minimum lockable signal level of −89 dBm at a voltage gain of 29 dB. Fig. 5 shows the phase noise of the unlocked ILFD at 1.2 GHz, in which the measured phase noise at 1 MHz offset is −105 dBc/Hz.

The proposed receiver exhibits an input 1 dB compression point of −25 dBm. Its sensitivity is evaluated using a Gaussian FSK (GFSK) signal with data rates of 1 and 2 Mb/s. Fig. 6 plots the measured BER performance at these data rates. The sensitivity for a BER of 10^{-3} at a data rate of 1 and 2 Mb/s is −83 and −80 dBm, respectively. Fig. 7 displays a clear eye diagram with a low peak-to-peak jitter while the receiver demodulates a received 2.4 GHz GFSK signal at a data rate of 1 Mb/s and an input power of −70 dBm. Table I compares the sensitivity and power consumption performance of this work with that of previous ILO- or PLL-based designs for 2.4 GHz GFSK receivers [4], [9], [10]. Obviously, the proposed receiver outperforms the others in reducing power consumption while providing comparable sensitivity.

V. CONCLUSION

In this letter, a 2.4 GHz CMOS FSK receiver based on a divide-by-2 ILFD and a single-balanced SHM is presented. The ILFD uses a ring oscillator to achieve large locking range and low power consumption. Moreover, the SHM provides a high LO-to-RF isolation to prevent the dc offset. The presented receiver can therefore be highly sensitive and energy-efficient. Measurement results exhibit a sensitivity of −83 dBm and a dissipated power of 1.1 mW when the receiver is used to detect a GFSK signal with a data rate of 1 Mb/s.

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